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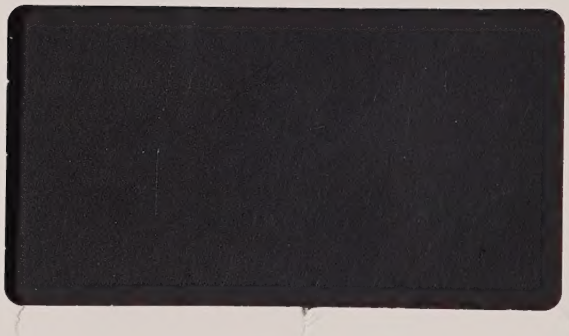

INSTRUCTION MANUAL

MODEL 175
ARBITRARY
WAVEFORM GENERATOR

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CONTENTS

SECTION 1 GENERAL DESCRIPTION

1.1 THE MODEL 175 1-1
1.2 SPECIFICATIONS 1-1
1.2.1 Versatility 1-1
1.2.2 Timing Precision 1-2
1.2.3 Amplitude Precision 1-2
1.2.4 General 1-2

SECTION 2 INSTALLATION AND INTERFACE

2.1 MECHANICAL INSTALLATION 2-1
2.2 ELECTRICAL INSTALLATION 2-1
2.2.1 Power Connection 2-1
2.2.2 Signal Connections 2-1
2.2.3 General Purpose Instrument Bus (GPIB) Connections 2-2
2.2.4 GPIB Address 2-2
2.2.5 Initial Checkout and Operation Verification 2-3
2.2.6 Permanent Custom Waveforms 2-3

SECTION 3 OPERATION

3.1 GENERAL 3-1
3.2 KEYBOARD 3-6
3.2.1 Notes 3-6
3.2.2 Key Descriptions 3-6
3.3 POWER 3-9
3.4 INPUTS AND OUTPUTS 3-9
3.5 BASIC COMMAND STRUCTURE 3-10
3.6 COUNTER GENERATED WAVEFORMS 3-12
3.7 MEMORY DATA (Y) FOR ARBITRARY WAVEFORMS 3-12
3.8 SMOOTHING (O) 3-12
3.9 SAMPLE TIME (T) AND WAVEFORM SMOOTHING 3-13
3.10 CLOCK TIME UNITS (S) 3-13
3.11 FULL OR PARTIAL BLOCK (U) 3-13
3.12 BLOCK RATE (F) 3-14
3.13 AMPLITUDE (A) AND OFFSET (D) 3-14
3.14 ERRORS 3-15
3.15 PRESET AND MONITOR TRIGGER (M) 3-16
3.16 GPIB 3-16
3.16.1 Bus Lines Defined 3-16
3.16.2 GPIB Commands 3-17
3.16.3 GPIB Data Transfers 3-18
3.16.4 GPIB Talk Message and Terminator Character (R) 3-18
3.16.5 GPIB Service Request Enable (Q) 3-19
3.17 INPUT AND OUTPUT IMPEDANCES 3-20
3.17.1 Arbitrary Waveform Outputs 3-20
3.17.2 TTL Outputs 3-20
3.17.3 TTL Inputs 3-20
3.17.4 Changing Source Impedance of the Main Output 3-20

CONTENTS (Continued)

SECTION 4 CALIBRATION

4.1 INTRODUCTION 4-1
4.2 TEST EQUIPMENT 4-1

SECTION 5 CIRCUIT DESCRIPTION

5.1 BOARD FUNCTIONS AND CONNECTIONS 5-1
5.2 GENERATOR 5-1
5.2.1 General 5-1
5.2.2 Generator Circuits 5-3
5.3 DISPLAY AND KEYBOARD 5-15
5.3.1 Display 5-15
5.3.2 Keyboard 5-17
5.4 MICROPROCESSOR 5-17
5.5 MICROPROCESSOR/GPIB INTERFACE 5-23
5.5.1 Data Ready 5-23
5.5.2 GPIB Busy 5-23
5.5.3 End 5-23
5.5.4 Remote 5-23
5.5.5 Talk 5-23
5.5.6 Listen 5-24
5.5.7 Service Request 5-24

SECTION 6 TROUBLESHOOTING

6.1 INTRODUCTION 6-1
6.2 POWER SUPPLY 6-1
6.3 FRONT PANEL DISPLAY 6-2
6.4 MICROPROCESSOR 6-4
6.5 GPIB INTERFACE 6-6
6.5.1 Test 1 — Bus Hung Up 6-6
6.5.2 Test 2 — Handshake 6-9
6.5.3 Test 3 — Listen Mode 6-10
6.5.4 Test 4 — Talk Address 6-11
6.5.5 Test 5 — Talk Mode 6-11
6.6 GENERATOR 6-12

SECTION 7 PARTS AND SCHEMATICS

7.1 DRAWINGS 7-1
7.2 ORDERING PARTS 7-1
7.3 ERRATA 7-1

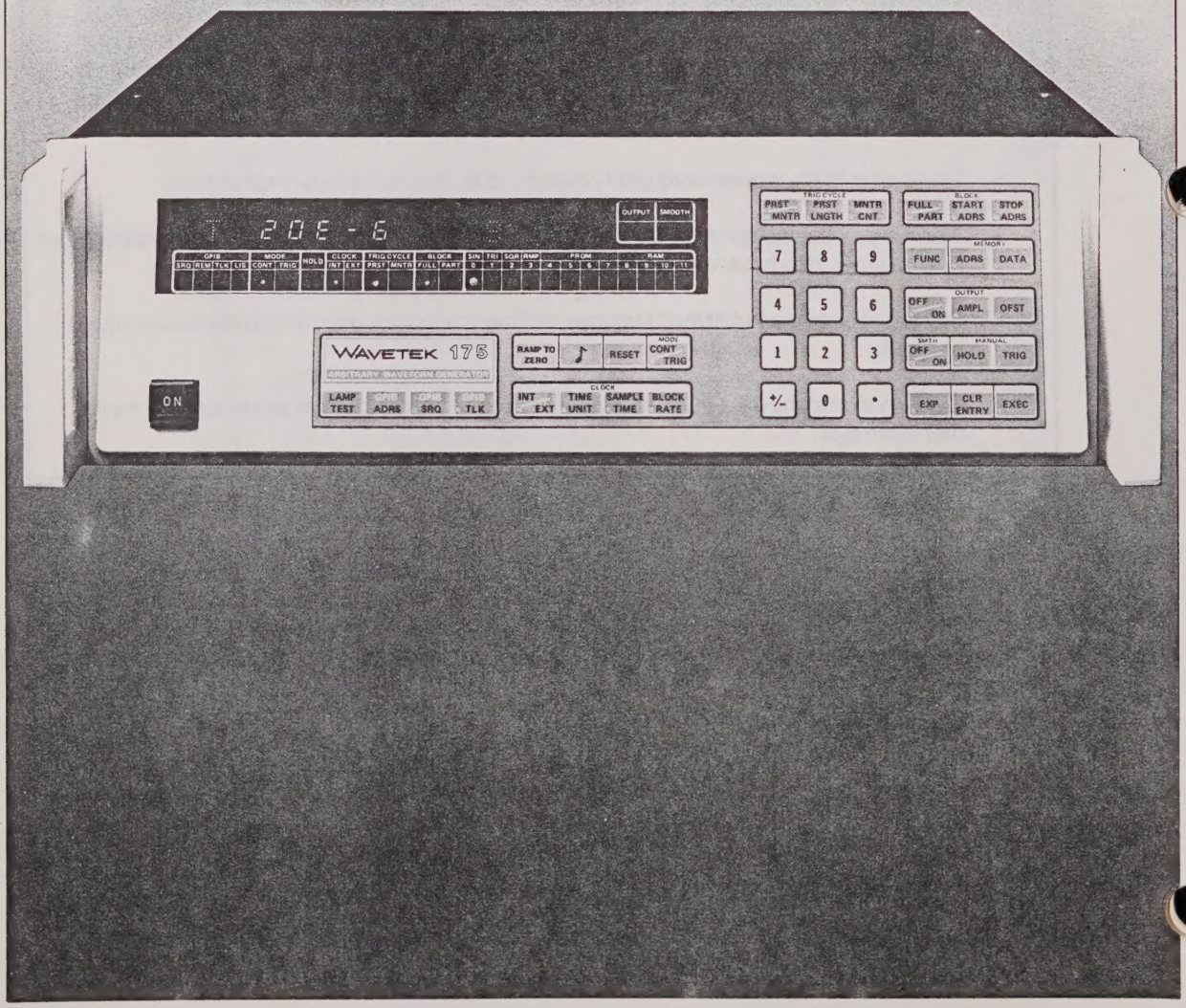
APPENDIX

APPENDIX A American Standard Code for Information Interchange (ASCII) A-1
APPENDIX B Programming Examples B-1
APPENDIX C Permanent Custom Waveforms C-1

SAFETY FIRST

Protect yourself. Follow these precautions:

- Don't touch the outputs of the instrument or any exposed test wiring carrying the output signals. This instrument can generate hazardous voltages and currents.
- Don't bypass the power cord's ground lead with two-wire extension cords or plug adaptors.
- Don't disconnect the green and yellow safety-earth-ground wire that connects the ground lug of the power receptacle to the chassis ground terminal (marked with ⏚ or ⚠).
- Don't hold your eyes extremely close to an rf output for a long time. The normally nonhazardous low-power rf energy generated by the instrument could possibly cause eye injury.
- Don't plug in the power cord until directed to by the installation instructions.
- Don't repair the instrument unless you are a qualified electronics technician and know how to work with hazardous voltages.
- Pay attention to the **WARNING** statements. They point out situations that can cause injury or death.
- Pay attention to the CAUTION statements. They point out situations that can cause equipment damage.



Model 175 Arbitrary Waveform Generator

SECTION 1
GENERAL DESCRIPTION

1.1 THE MODEL 175

The Model 175, Arbitrary Waveform Generator (Arb), generates any waveform that can be expressed as a function of time. The working Random Access Memory (RAM) has four sets of 256 addresses and each address accepts an 8 bit word. This corresponds to a 1024 (time) by 255 (amplitude) matrix in which to draw waveforms. These storage addresses can be manually loaded by front panel controls or remotely loaded via the GPIB interface. The stored waveform, or any portion thereof, then can be generated at selectable clock rates and amplitudes.

In addition to the four working Random Access Memories (RAMs), four optional Programmable Read Only Memories (PROMs) allow the same capacity for permanent waveform storage. Sine, triangle, square and ramp waveforms are always available.

Operation can be continuous or triggered. Triggering can be for a preset number of cycles or the number of cycles triggered can be monitored and displayed. Start and stop addresses are selectable for partial waveform output. At low frequencies, point-to-point smoothing can be selected to minimize digital step size. Output may be held at any level, or amplitude and offset can be slowly ramped to zero when a ramp to zero command is given.

Front panel operation is by keyboard and display which gives immediate verification of parameter and value in memory.

The Model 175 is fully compatible with the requirements of IEEE Standard 488-1975 for integration into a General Purpose Interface Bus (GPIB).

1.2 SPECIFICATIONS

1.2.1 Versatility

1.2.1.1 Waveforms

Sine ∿, square ⊓, triangle △, ramp ◿, arbitrary waveforms and TTL sync. (See figure 1-1.)

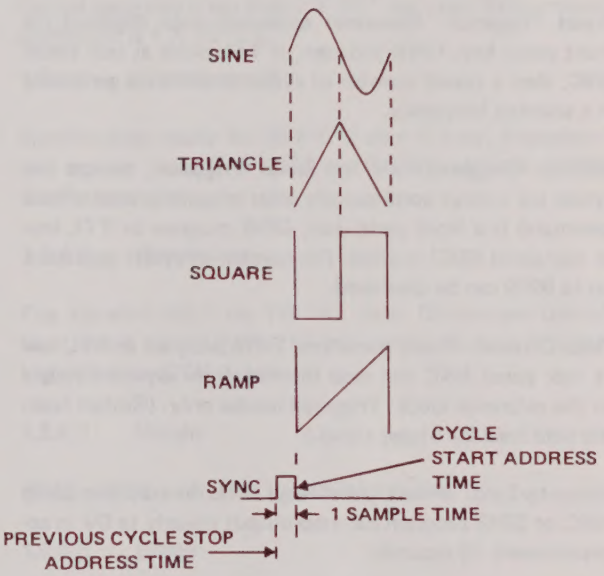


Figure 1-1. Fixed Waveforms

1.2.1.2 Arbitrary Waveforms

Arbitrary waveforms are stored on four 256 X 255 point RAM matrices and four 256 X 255 user-supplied PROM matrices. Each PROM or RAM block can be addressed individually or they can be addressed in sequence; e.g., PROMs 1 and 2, PROMs 1, 2 and 3 or PROMs 1, 2, 3 and 4. This feature allows additional address resolution of custom waveforms. Block length can be from 2 to 256 address points, or when blocks are stacked, up to 1024 address points.

1.2.1.3 Digital Smoothing

When smoothing is selected, each change in amplitude data is subdivided into 100 substeps per sample time. Smoothing is automatically limited to 20 μs or slower sampling times and to point-to-point data differentials less than 64.

1.2.1.4 Sync Output

TTL level pulse with a trailing edge coincident with the start address. Pulse width is one sample time. Available at rear panel BNC.

1.2.1.5 Cursor Output

TTL level output coincident with a selected data address. Available at rear panel BNC.

1.2.1.6 Operational Modes

Continuous: Generator operates continuously at selected frequency.

Preset Triggered: Generator quiescent until triggered via front panel key, GPIB program or TTL pulse at rear panel BNC; then a preset number of cycles to 9999 are generated at a selected frequency.

Monitor Triggered: As for Preset Triggered, except the cycles are output continuously after triggering, until a hold command (via front panel key, GPIB program or TTL low at rear panel BNC) is given. The number of cycles generated up to 9999 can be displayed.

Hold Control: Front panel key, GPIB program or TTL low at rear panel BNC can stop the waveform asynchronously to the reference clock. Triggered modes only. (Restart from the held level by trigger signal.)

Ramp-to-Zero: Front panel key, TTL low at rear panel BNC or GPIB program can step output linearly to 0V in approximately 15 seconds.

1.2.2 Timing Precision

1.2.2.1 Sample Time

The stepping time from data point to adjacent data point is selectable as 200 ns to 999.9s for fixed waveforms and optional PROM stored data points (500 ns to 999.9s for RAM stored data points). Sample time accuracy is ±0.03% of setting. Resolution is 100 ns (10 μs when smoothing). Output frequency is 19.5 kHz to 3.90 μHz (71 hr/cycle) rate for a 256 word block. Sample time can be displayed and programmed in seconds, minutes, hours or as data block rate in hertz.

1.2.2.2 Reference Clock

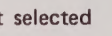
Internal 10 MHz crystal controlled oscillator or external TTL compatible frequency source input at rear panel BNC. TTL compatible reference clock output provided.

1.2.2.3 External Clock

TTL compatible signal applied at rear panel BNC. Permissible external clock frequency is dc to 11 MHz for continuous modes. Ratio of external clock to reference clock determines output frequency.

1.2.3 Amplitude Precision

1.2.3.1 Main Output (Attenuated, 50Ω Source)

 and arbitrary waveform selectable. Full block amplitude variable from 2 mV to 20V peak-to-peak into open circuit (10V peak-to-peak into 50Ω) with 3 digit resolution. Amplitude accuracy with 0 Vdc offset between 2 and 20V p-p is ±2% of setting plus 2 digits. Signal offset is from 0 to ±10V into open circuit (0 ±5V into 50Ω) with 3 digit resolution. Offset accuracy is ±2% of setting plus 2 digits.

1.2.3.2 Auxiliary Output (<1Ω Source)

Same waveform as main output from 0 to 10V peak (at fixed 0 dB attenuation). Same offset as main output and limited to 100 mA peak.

1.2.3.3 Output Amplifier Rise/Fall Time

Less than 500 ns, 50Ω termination, main output.

1.2.4 General

1.2.4.1 Display

LED seven segment display with alphabetical index of key functions and units. All status, modes and functions are shown by LED annunciator displays.

1.2.4.2 Keyboard

Membrane type with acoustic feedback. Acoustic tone may be turned off by front panel key.

1.2.4.3 External Program Interface

IEEE Standard 488-1975 compatible General Purpose Interface Bus (GPIB). Connector and address switch on rear panel. The interface provides listener (AH1 and L4), talker (SH1 and T6), service request (SR1), remote/local (RL1), device clear (DC1) and device trigger (DT1) capabilities. Handshake rate is 2 μs per character in command mode (10 μs typical for command sequence) and 220 μs per character in data mode, with data storage of up to 80 characters. The following table may be used to determine particular through-put times. Measurements were made with a 175 and an HP9825 controller. Data rates will follow

the slowest listener on the bus and vary with different controllers.

Parameter	Time
Command Handshake	2 μs
Data Handshake	220 μs
Sample Time	35 ms
Block Rate	50 ms
Amplitude Setting	65 ms
DC Offset Setting	65 ms
Burst Length	20 ms
Function	20 ms
Int/Ext Clock	20 ms
Time Unit	25 ms
Mode CONT/TRIG	20 ms
PRST/MNTR Trigger	20 ms
FULL/PART Block	25 ms
Start Address	25 ms
Stop Address	25 ms
Output OFF/ON	20 ms
X Address	30 ms
Y Data	40 ms
Smoothing OFF/ON	35 ms
Execute	16 ms*
GET	1.6 ms

**2 ms when via GET*

1.2.4.4 Stability

Amplitude and DC Offset
Measured at full output and 25 ±1°C. Change is less than ±0.25% per day. Change with temperature is less than ±0.2% over 0 to 50°C.

Frequency
Crystal aging rate is less than 2×10^{-5} per year. Temperature coefficient is 1×10^{-6}/°C.

1.2.4.5 Environmental

Specifications apply for 25 ±10°C after ½ hour. Instrument will operate from 0 to 50°C to 10,000 ft altitude at 95% relative humidity.

1.2.4.6 Dimensions

Fits standard 48.3 cm (19 in.) rack. Dimensions behind front panel are 43.2 cm (17 in.) wide; 13.3 cm (5¼ in.) high; 51.4 cm (20¼ in.) deep.

1.2.4.7 Weight

15.9 kg (35 lb) net; 20.4 kg (45 lb) shipping.

1.2.4.8 Power

90 to 105V, 108 to 126V, 198 to 231V or 216 to 252V; 48 to 66 Hz; less than 120 watts.

SECTION 2
INSTALLATION AND INTERFACE

2.1 MECHANICAL INSTALLATION

After unpacking the instrument, visually inspect all external parts for possible damage to connectors, surface areas, etc. If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing material should be saved in case reshipment is required.

The generator can be used as a bench instrument or rack mounted. In either use, ensure that there is no impedance to air flow at any surface of the instrument.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

NOTE

Unless otherwise specified at the time of purchase, this instrument was shipped from the factory with the power transformer connected for operation on a 120 Vac line supply and with a 2 amp fuse.

Conversion to other input voltages requires a change in rear panel fuse holder voltage card position and fuse (figure 2-1) according to the following procedure.

Card Position	Input Vac	Fuse
100	90 to 105	2 amp
120	108 to 126	2 amp
220	198 to 231	1 amp
240	216 to 252	1 amp

1. Disconnect the power cord at the instrument, open fuse holder cover door and rotate fuse pull to left to remove the fuse.
2. Remove the small printed circuit board and select operating voltage by orienting the printed circuit board to position the desired voltage to the top left side. Push the board firmly into its module slot.
3. Rotate the fuse-pull back into the normal position and insert the correct fuse into the fuse holder. Close the cover door.
4. Connect the ac line cord to the mating connector at the rear of the unit and the power source.

2.2.2 Signal Connections

Use RG58U 50Ω shielded cables equipped with BNC connectors to distribute signals (figure 2-1) when connecting this instrument to associated equipment.

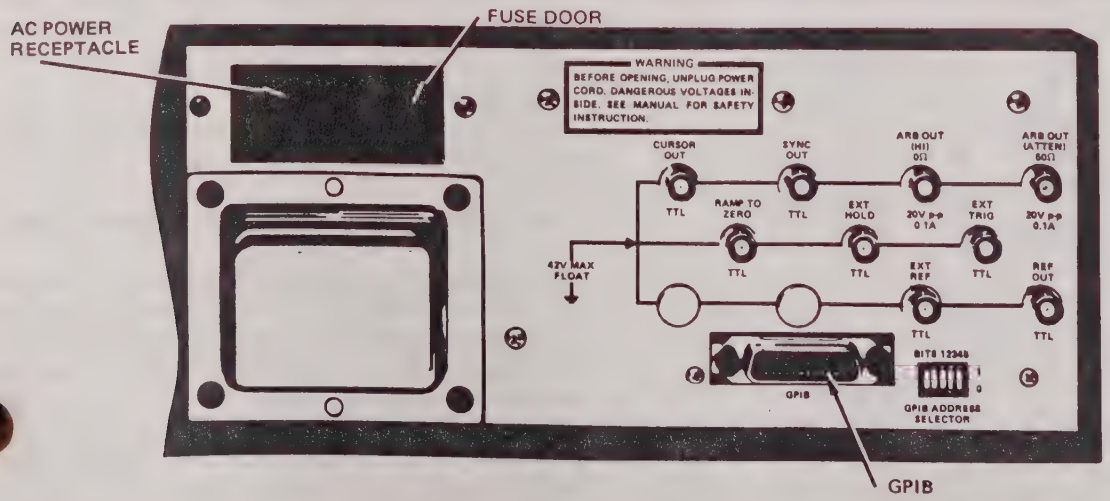


Figure 2-1. Rear Panel

2.2.3 General Purpose Interface Bus (GPIB) Connections

The GPIB I/O rear panel connection is shown in figure 2-1; pin connections and signal names are given in table 2-1. The panel connector is an Amphenol 57-10240 or equivalent and connects to a GPIB bus cable (available from Wavetek). The GPIB interface is optically isolated from the instrument.

2.2.4 GPIB Address

For instruments on the GPIB, ensure that the GPIB address is correct.

The GPIB address can be changed by the switch on the rear of the instrument (see figure 2-1) by simply setting the multiple section switch according to table 2-2. The switch sections are labeled from 1 through 5 and their open position noted (OPEN = "0" in table 2-2). To verify the address, press GPIB ADR on the front panel. The device number (decimal) will be displayed as "0, 1, — 30."

Table 2-1. GPIB Data In/Out

Pin	Signal	
1	DIO1	True When Low
2	DIO2	
3	DIO3	
4	DIO4	
5	EOI	
6	DAV	
7	NRFD	True When High
8	NDAC	
9	IFC	True When Low
10	SRQ	
11	ATN	
12	Safety Gnd	
13	DIO5	True When Low
14	DIO6	
15	DIO7	
16	DIO8	
17	REN	
18		Signal Gnd
19		
20		
21		
22		
23		
24		

Table 2-2. GPIB Address Codes

	Address								
	ASCII		Switch Position					Hexa-decimal	
Device	Listen	Talk	1	2	3	4	5	Listen	Talk
0	(space)	@	0	0	0	0	0	20	40
1	!	A	1	0	0	0	0	21	41
2	"	B	0	1	0	0	0	22	42
3	#	C	1	1	0	0	0	23	43
4	$	D	0	0	1	0	0	24	44
5	%	E	1	0	1	0	0	25	45
6	&	F	0	1	1	0	0	26	46
7	'	G	1	1	1	0	0	27	47
8	(	H	0	0	0	1	0	28	48
9	)	I	1	0	0	1	0	29	49
10	*	J	0	1	0	1	0	2A	4A
11	+	K	1	1	0	1	0	2B	4B
12	,	L	0	0	1	1	0	2C	4C
13	—	M	1	0	1	1	0	2D	4D
14	•	N	0	1	1	1	0	2E	4E
15	/	O	1	1	1	1	0	2F	4F
16	0	P	0	0	0	0	1	30	50
17	1	Q	1	0	0	0	1	31	51
18	2	R	0	1	0	0	1	32	52
19	3	S	1	1	0	0	1	33	53
20	4	T	0	0	1	0	1	34	54
21	5	U	1	0	1	0	1	35	55
22	6	V	0	1	1	0	1	36	56
23	7	W	1	1	1	0	1	37	57
24	8	X	0	0	0	1	1	38	58
25	9	Y	1	0	0	1	1	39	59
26	:	Z	0	1	0	1	1	3A	5A
27	;	[	1	1	0	1	1	3B	5B
28	<	\	0	0	1	1	1	3C	5C
29	=	]	1	0	1	1	1	3D	5D
30	>	↑	0	1	1	1	1	3E	5E

2.2.5 Initial Checkout and Operation Verification

The equipment and procedures in tables 2-3 and 2-4 are recommended for incoming inspection and for testing the instrument after repair. However, additional after repair tests or calibration (Section 4) may be necessary for certain circuits.

Operation verification includes the following procedures.

1. **Power On:** Verifies initial conditions as determined by microprocessor and firmware circuits.

2. **Lamp Test:** Verifies condition of display lamps.

3. **Output Waveform Test:** Sine wave output is visually checked for correct frequency and visible irregularities. Smoothing also checked.

4. **Function Test:** Verifies standard waveforms.

5. **Waveform Generation Test:** Verifies data may be entered and appropriate waveform generated.

6. **Ramp To Zero Test:** Verifies ramp to zero operation.

7. **Reset Test:** Verifies proper resetting of instrument.

8. **Amplitude Accuracy Test:** Verifies amplitude accuracy of dc and ac operations.

9. **Frequency Accuracy Test:** Verifies block rate accuracy.

10. **Interface Test:** Verifies remote control capabilities of listening and talking.

Before making an initial checkout, review power and signal connection requirements (paragraphs 2.2.1 and 2.2.2) and ensure the availability of test equipment equivalent to that listed in table 2-3. An acceptance test record sheet (table 2-5) may be reproduced for recording checkout test results.

2.2.6 Permanent Custom Waveforms

Four 74S471 PROMs containing custom waveform data may be added in socket positions U7E through U10E on the generator board 1100-00-0644 (drawing 0101-00-0644).

Refer to Appendix C for PROM encoding and to paragraph 3.2.2(19) for operator access to these waveforms.

Table 2-3. Equipment Required for Incoming Inspection and Operation Verification

Instrument	Critical Specifications	Model Recommended
Oscilloscope	≥30 MHz vertical bandwidth	Tektronix 7903
50Ω Load	BNC feedthru	Tektronix 011009900
Voltmeter	0.1 to 10V ranges 3 digit resolution ±0.1% accuracy	Dana 6000 Series
Frequency Counter	20 MHz capability 5 digit resolution ±0.01% accuracy	Dana 9000 Series
Calculator	IEEE 488-1975 compatible	HP9825

Table 2-4. Operation Verification

Step	Test	Tester and Setup	Program	Desired Results
1	Power On	None.	Power ON	Several LEDs light momentarily, then darken, with only the following remaining lit: MODE — CONT; CLOCK — INT; TRIG CYCLE - PRST; BLOCK — FULL; Function — SIN 0.
2	Lamp Test	None.	LAMP TEST	All display LEDs lit. The last three 8's are not followed by decimal points.

Table 2-4. Operation Verification (Continued)

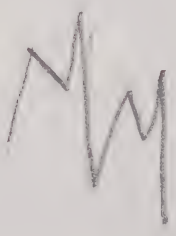
Step	Test	Tester and Setup	Program	Desired Results
3	Output Waveform	Oscilloscope. Connect ARB OUT (ATTEN) 50Ω with 50Ω load at the scope input. Set for 2 V/div, horizontal 1 ms/div, external auto trigger. Connect ARB SYNC OUT to scope external trigger input.	OUTPUT OFF/ON 1 AMPL 10 SMTH: OFF/ON 1 EXEC	Approximately 5 div per cycle, 10V p-p visually nondistorted sine wave.
4		Oscilloscope. Set horizontal for .02 ms/ div.		Nearly straight line (expanded sine curve) on scope.
5			SMTH OFF/ON 0 EXEC	Stair step waveform on scope.
6		Oscilloscope. Set horizontal for 1 ms/div.		Sine waveform on scope.
7	Function		FUNC 1 EXEC	Triangle waveform on scope.
8			FUNC 2 EXEC	Square waveform on scope.
9			FUNC 3 EXEC	Ramp waveform on scope.
10	Waveform Generation		SMTH 1 FUNC 8 EXEC MEMORY: ADRS 0 DATA 0 ADRS 50 DATA 127 ADRS 100 DATA −127 ADRS 150 DATA +35 ADRS 255 DATA 0 EXEC	Triangle waveform followed by dow slope ramp waveform on scope. 
11	Ramp To Zero	Oscilloscope. Set horizontal to .2s/div. Adjust scope intensity to safe level.	BLOCK RATE .1 EXEC	Trace moves slowly across scope.
12			Depress RAMP TO ZERO key when scope trace is near a + or − peak on waveform.	HOLD LED lights. Trace changes desired waveform to a ramp that slowly approaches zero. The ARB display indicates a 'G' within 15 seconds.
13	Reset		EXEC	Trace same as in step 11.
14		Oscilloscope. Set horizontal for .02 ms/ div.	RESET	Scope display is 0 volts. The following LED display indicators are lit: MODE — CONT; CLOCK — INT; TRIG CYCLE — PRST; BLOCK — FULL; FUNCTION — SIN 0.

Table 2-4. Operation Verification (Continued)

Step	Test	Tester and Setup	Program	Desired Results
15		Oscilloscope. Set horizontal for 1 ms/div.	OUTPUT: OFF/ON 1 AMPL 10 SMTH: OFF/ON 1 EXEC	Visually nondistorted sine wave.
		NOTE: Allow 30 minute warm-up before performing the following tests.		
16	Amplitude Accuracy	(Disconnect oscilloscope.) Voltmeter. Set to Vrms, ac. Connect to ARB OUT (ATTEN) 50Ω with a precision 50Ω load at voltmeter input.		3.35 to 3.71 Vrms.
17		Voltmeter. Set to read Vdc.	AMPL 0 OFST 5 EXEC	+4.75 to +5.25 Vdc.
18	Frequency Accuracy	(Disconnect voltmeter.) Counter. Set to read frequency nominal 200 Hz at 10V p-p input. Connect to ARB OUT (ATTEN) 50Ω with 50Ω load at counter input.	AMPL 5 OFST 0 EXEC FUNC 2	192 to 198 Hz.
19	Interface	Oscilloscope. Connect ARB OUT (ATTEN) 50Ω with 50Ω load at the scope input. Set trigger to ext, dc, normal. Calculator. Connect to ARB GPIB connector. Set ARB rear panel GPIB ADDRESS SWITCH to 00100. Press GPIB ADRS key and verify GPIB address is "4" on display.	Calculator: 0: dim A$[100] 1: fxd 2 2: wrt 704,"ZI" 3: wait 1000 4: wrt 704, "A5O1 P1I" 5: stp	10V p-p sine wave of 5.12 ms period.
20			6: wrt 704,"C11I X100Y-127X153Y1 27X154Y-127IB1D 0M0L3U1V100W154 T5E-6I" 7: wait 500 8: for I=1 to 20 9: wait 500 10: trg 704 11: next I 12: stp	20 bursts of 3 partial ramp waveforms in approximately 0.5s intervals.
21			13: wrt 704,"ZI" ;wait 1000 14: wrt 704,"R3I F" 15: red 704,A$ 16: prt A$;stp 17: lcl 704 18: prt "175 test complete" 19: stp	Calculator printout. V F 195.31

Table 2-5. Acceptance Test Record
(for reproduction)

Location _____

QA Inspector _____

Date _____

Instrument S/N _____

		Acceptable (✓)
A.	Manual Checks, Data Entry and Visual Checks (steps 1 through 15)	_____
B.	Amplitude Accuracy	
	(step 16) _____ Vrms	_____
	(step 17) _____ Vdc	_____
C.	Frequency Accuracy	
	(step 18) _____ Hz	_____
D.	Interface-GPIB (steps 19 through 21)	_____

SECTION 3
OPERATION

3.1 GENERAL

The waveforms to be output are contained as a series of values in storage, which are read and output at some selected rate. There are 12 blocks each of 256 addresses (4 blocks are optional). Four blocks have fixed waveforms of sine, triangle, square and ramp, respectively. For example, in the sine wave block, the values for each address determine 256 data points that approximate the shape of a sine wave. Four optional PROM blocks each contain custom waveforms. Four RAM blocks may be loaded with waveform data and erased, as required.

The selected block of waveform may be output from address zero to address 255 (one cycle) repeatedly to form a continuous waveform output. As a variation, any start address and any stop address may be specified for the cycle. Or, two, three or four blocks may be linked together for one cycle of the output waveform. Blocks that can be linked are PROM blocks 1 and 2; 1, 2 and 3; 1, 2, 3 and 4. Similarly, the RAM blocks may be linked. The dwell time at each address, the time the output is the value for that address, can be selected as either sample time (in seconds, minutes or hours) or block rate (in Hertz).

Besides the continuous output of a waveform, triggered output may be selected. A preset number of cycles may be output when the Arb is triggered. Or, when triggered, the output waveform can be continuous until stopped by a Hold command. The number of cycles output can then be read by a Monitor Count command.

The waveform amplitude may be dc offset, attenuated and smoothed. Smoothing minimizes the transition between amplitude steps for amplitude step differences less than 64.

The 50Ω output is off at power on time, which allows programming before electrically connecting the Arb output to the outside world. To change the output, the change must be programmed or keyed and then executed by an Execute command or pressing the EXEC key. An example of front panel operation is given in table 3-1.

Table 3-1. Example of Front Panel Data Entry

Instruction	Front Panel Entry (Press Keys)	Equivalent Program	Front Panel Display
1. Power on. The display shows most of the initial conditions.	[OFF] (becomes [ON])		See figure 3-1.
2. Test lamps. (27 status lamps, a 5 X 7 dot matrix, four 8's with decimals, three 8's without decimals and an asterisk.	[LAMP TEST]		All lamps should be lit.
3. Check initial conditions at every key.	Press each front panel key		See paragraph 3.2
4. Connect an oscilloscope to the ARB OUT (ATTEN) 50Ω connector using a 50Ω load. Enable the output and observe the sine waveform.	OUTPUT [OFF/ON] [1] [EXEC]	P1 I	P1 I [OUTPUT •]
5. Use the oscilloscope to amplify the waveform until the individual steps of the waveform can be seen. Smooth the waveform.	SMTH [OFF/ON] [1] [EXEC]	O1 I	O1 I [SMOOTH •]

Table 3-1. Example of Front Panel Data Entry (Continued)

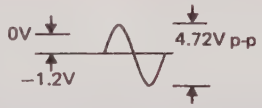
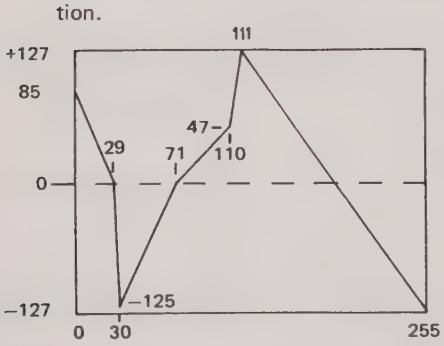
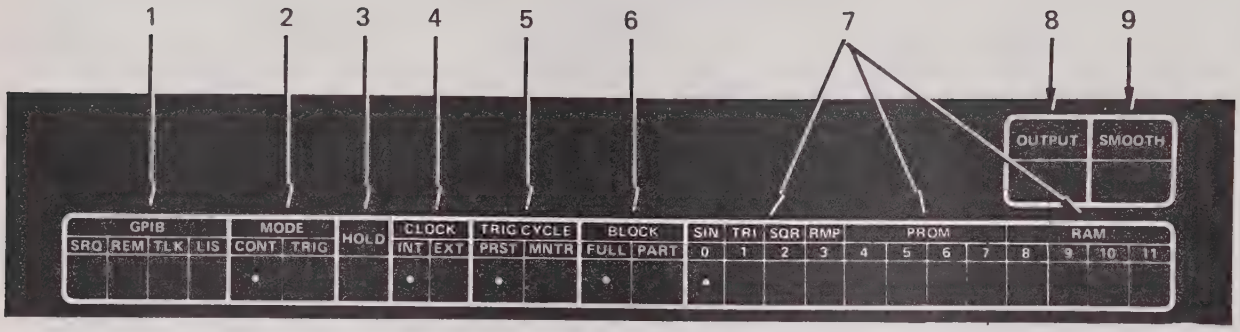
Instruction	Front Panel Entry (Press Keys)	Equivalent Program	Front Panel Display
6. Change the amplitude and offset to: 	AMPL 4 • 7 2	A4.72	A4.72
	OFST +/− 1 • 2	D−1.2	D−1.2
	EXEC	I	I
7. Oberserve the other waveforms. (There may be no waveforms in C4 thru C7.) C8 thru C11 will have a 0V baseline.	FUNC 1	C1	C1
	EXEC	I	I TRI 1 •
	FUNC 2	C2	C2
	EXEC	I	I SQR 2 •
	FUNC 3	C3	C3
	EXEC	I	I RMP 3 •
	FUNC 4	C4	C4
	EXEC	I	I PROM 4 •
	(etc. to C11)		
8. Design a simple waveform in C11. This illustrates the use of automatic interpolation.  A line is drawn to the plotted point when the following ADR key is pressed.	ADRS 0	X0	X0
	DATA 8 5	Y85	Y85
	ADRS 2 9	X29	X29
	DATA 0	Y0	Y0
	ADRS 3 0	X30	X30
	DATA +/− 1 2 5	Y−125	Y−125
	ADRS 7 1	X71	X71
	DATA 0	Y0	Y0
	ADRS 1 1 0	X110	X110
	DATA 4 7	Y47	Y47
	ADRS 1 1 1	X111	X111
	DATA 1 2 7	Y127	Y127
	ADRS 2 5 5	X255	X255
	DATA +/− 1 2 7	Y−127	Y−127
9. Observe this waveform on the oscilloscope.	EXEC	I	I

Table 3-1. Example of Front Panel Data Entry (Continued)

Instruction	Front Panel Entry (Press Keys)	Equivalent Program	Front Panel Display
10. Select only one portion of this waveform and observe it on the oscilloscope. (Frequency increases because there are less data points being sampled. The sampling rate has remained the same.)	FULL/PART 1	U1	U1
	START ADRS 2 0	V20	V20 BLOCK FULL PART •
	STOP ADRS 1 1 1	W111	W111
	EXEC	I	I
11. Prepare to output exactly 321 cycles of this waveform.	CONT/TRIG 1	B1	B1
	PRST/MNTR 0	M0	M0
	PRST LNGTH 3 2 1	L321	L321
	EXEC	I	I
12. When triggering, observe the Hold status light.	TRIG	J	J HOLD then HOLD •
13. Return to full block mode.	FULL/PART 0	U0	U0
14 Change the frequency to approximately 10 kHz.	BLOCK RATE 1 0 E 3	F10E3	F10E3
	EXEC	I	I
15. Examine the actual sample time.	SAMPLE TIME	T	T400E−9 S
16. Examine the actual frequency.	BLOCK RATE	F	F9.7656E3 Hz

NOTE: Frequency is determined by the number of blocks stacked, the number of data points in a cycle and the sample time per data point. Therefore, desired frequencies can only be approximate.

$$\textit{Actual Frequency} = \frac{1}{\textit{(Sample Time) (No. of Data Points in a Block) (Number of Blocks Stacked)}}$$



1. **GPIB Status:**
   - SRQ — Service request being sent
   - REM — Remote (GPIB) control
   - TLK — Arb talking on the GPIB
   - LIS — Arb listening on the GPIB

   } if lit

2. **Mode Status:** Continuous or triggered output.

3. **Hold Status:** Output is being held at some data point if lamp is lit.

4. **Clock Status:** Internal 10 MHz clock or external clock (11 MHz maximum).

5. **Triggered Cycle Status:** Preset number of cycles or monitor the number of cycles output.

6. **Block Status:** The full block or a partial block of data points is being used.

7. **Function Status:** Sine, triangle, square, ramp, PROM stored or RAM stored waveform output. The lamp of the selected block is lit. If multiple blocks of RAM or of PROM are being stacked together, then the lamps of the stacked blocks are lit.

8. **Output Status:** Output on if lamp is lit.

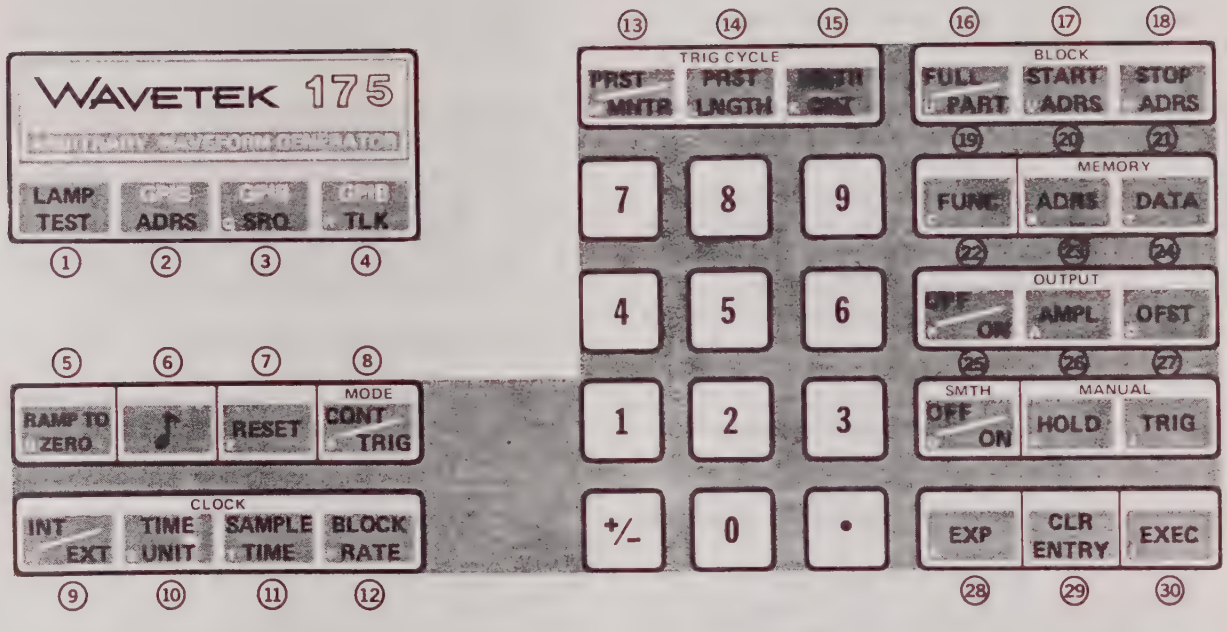
9. **Smoothing Status:** Smoothing of digital waveform steps active if lamp is lit.

NOTES:

"Power On" condition shown:

1. *Local Control — Not GPIB (Remote Control)*
2. *Continuous Mode*
3. *Generator Running*
4. *Internal Clock*
5. *Preset Number of Triggered Cycles (however, mode is continuous)*
6. *Full Block of 256 Data Points Used*
7. *Sine Waveform*
8. *Output Off*
9. *Smoothing Off*

Figure 3-1. Status Display



NOTE: See paragraph 3.2 for item descriptions

Figure 3-2. Keyboard

3.2 KEYBOARD

3.2.1 Notes

1. Most keys (figure 3-2) are associated with a parameter and, when pressed, give the status of that parameter. The parameter status or value is changed by pressing number keys after the parameter key. Other keys give immediate action when pressed.

2. The key functions that can be GPIB programmed have their GPIB ASCII character in the lower left corner and are called alpha keys. (The block of number keys may also be programmed.)

3. Because of the variety of format that the operator can use when entering values, the microprocessor does not assume that programming is complete until another alpha key (except EXP) is pressed. At this time, the value is tested and, if ok, placed in a scratch pad memory.

4. When an asterisk (*) appears in the display, it indicates that a number is being entered from either the keyboard or GPIB.

5. Initial conditions (*I/C*) at power-on time are noted in paragraph 3.2.2.

6. Brief key descriptions are given in paragraph 3.2.2. Details on the use of the keys are in the following paragraphs and referenced where applicable.

7. Errors detected are flagged by an "ERROR" in the display. Refer to paragraph 3.14.

3.2.2 Key Descriptions

The following item numbers correspond to those in figure 3-2.

1. **Lamp Test** — Lights all display status blocks and display segments.

2. **GPIB Address** — Shows GPIB decimal address set by switches on rear panel.

3. **GPIB Service Request Enable (Q)** — Shows what conditions will cause the Arb to send a service request over the GPIB:

   Q0 — Suppresses all service requests.
   Q1 — Enables service request for errors (*I/C*).
   Q2 — Enables service request when the waveform generation circuits make a transition from not holding to holding.
   Q3 — Enables service request for errors and transition to holding.

   Refer to paragraph 3-16 for related GPIB data.

4. **GPIB Talk (R)** — Shows the status of two parameters: The particular type of talk message that will be given when the Arb is addressed to talk over the GPIB is shown on the left of the display. A minus sign prefix and the decimal equivalent of the ASCII coded terminator character is shown on the right. The talk message codes are:

   R0 — State of hold status (returns "0" if not holding, "1" if holding (*I/C*).
   R1 — List of first nine errors since this message was last read.
   R2 — Reason why this instrument is requesting service.
   R3 — Current value of the setting, if any, selected by the last alphabetical character used.

   Refer to paragraph 3.16.4 for details.

5. **Ramp to Zero (G)** — An abort action that increments the amplitude and offset in linear steps to zero in about 15 seconds. The Arb does not respond to new inputs during ramping. "G" is not displayed until zero is reached. Press EXEC to restore prior status.

6. **Musical Note** — Key tone (*I/C*) is cut out or, if out, restored.

7. **Reset (Z)** — Sets everything to initial conditions except RAM storage (waveforms programmed are not lost as long as power is on). Initial conditions for items in paragraph 3.2.2 are annotated with (*I/C*).

   When programming this action via the GPIB, the controller should wait for the instrument to start resetting before sending any futher commands. If the instrument microprocessor is idle, a 3 millisecond wait will suffice, but if it is busy scanning an input buffer (refer to paragraph 3.16.3), the wait required could be as long as a second. The wait is necessary to avoid losing the commands following the reset command.

8. **Mode, Continuous or Triggered (B)** — Shows status:

   B0 — Continuous (*I/C*).
   B1 — Triggered.

   In continuous mode, the Arb continuously generates the selected waveform, and it cannot be triggered or held. In triggered mode, the Arb is idle until a trigger stimulus is received.

When a trigger (J) occurs, the Arb starts to generate the selected waveform until a hold (H) command is received or, if the trigger cycle parameter (M) is set to the preset mode, until the number of blocks specified by the preset length parameter (L) have been generated. Refer to item 13 and paragraph 3.15 for details.

9. **Clock, Internal or External (N)** — Shows source status:

N0 — Internal 10 MHz clock (*I/C*).
N1 — External clock (≤ 11 MHz).

This parameter selects the source of the clock which provides timing for the waveform generator circuits. If the external clock is selected, it must be within these limits:

dc - 11 MHz, if mode is continuous (B0)
500 kHz - 11 MHz, if mode is triggered (B1)

10. **Clock, Time Unit (S)** — Shows the units used for sample time:

S0 — Seconds (*I/C*)
S1 — Minutes
S2 — Hours

Refer to paragraph 3.10 for conditions that affect time unit.

11. **Clock, Sample Time (T)** — Shows duration of each data point of the output waveform.

Example: T20E−6s = 20 μs (*I/C*)

See paragraph 3.12 for conditions that affect sample time.

12. **Clock, Block Rate (F)** — Shows frequency of the output waveform.

Example: F195.313 Hz (*I/C*)

See paragraph 3.12 for conditions that affect block rate.

13. **Trigger Cycle, Preset or Monitor (M)** — Shows status:

M0 — Preset Mode (*I/C*). A preset number of cycles will be output following a trigger signal. (Refer to item 14.)
M1 — Monitor Mode. When triggered (J) output is continuous.

Refer to paragraph 3.15 for details.

14. **Trigger Cycle, Preset Length (L)** — Shows the number of waveform blocks generated when a trigger (J) is received in triggered mode (B0) with preset trigger cycle mode (M0) selected.

Example: L216 — When in preset mode (M0) and triggered (J), 216 cycles of waveform will be output. L1 (*I/C*)

15. **Trigger Cycle, Monitor Count (K)** — This is an interrogating action which reads the value of the triggered waveform cycle counter. If continuous mode (B0) is selected, the value readout is always zero. If triggered mode (B1) is selected, the value readout is the number of complete blocks generated since the generator was last triggered. While the generator is running (not holding), the cycle counter is incremented when the last point in a block is being output. When holding, the counter is not incremented. Refer to paragraph 3.15 for more details.

16. **Block, Full or Partial (U)** — Shows status:

U0 — A full 256 address block (or several blocks) forms one cycle of waveform (*I/C*).
U1 — A partial block forms one cycle. (Refer to items 17 and 18.)

Refer to paragraph 3.11 for operation.

17. **Block, Start Address (V)** — Shows block start address of waveform.

Example: V93 — One cycle of waveform starts at address 93 in 0 - 255 block. V0 (*I/C*)

18. **Block, Stop Address (W)** — Shows block stop address of waveform.

Example: W107 — One cycle of waveform stops at address 107 in 0 - 255 block. W255 (*I/C*)

19. **Function (C)** — Shows which memory (or memories) will be used to generate the output waveform. Values 0 - 3 select standard waveforms:

C0 — Sine (*I/C*)
C1 — Triangle
C2 — Square
C3 — Ramp

Values 4 - 7 select the four user-supplied PROM blocks.

C4 — PROM block 1
C5 — PROM block 2

C6 – PROM block 3
C7 – PROM block 4

Values 8 - 11 select the four programmable RAM blocks.

C8 – RAM block 1
C9 – RAM block 2
C10 – RAM block 3
C11 – RAM block 4

Values 14 - 17 select joined together, user-supplied PROM blocks. The PROMs composing these are the same ones that are selected by function codes 4 - 7.

C14 – PROM block 1 (256 points maximum)
C15 – PROM blocks 1 & 2 (512 points maximum)
C16 – PROM blocks 1, 2 & 3 (768 points maximum)
C17 – PROM blocks 1, 2, 3 & 4 (1024 points maximum)

Values 18 - 21 select joined together, programmable RAM blocks. The RAMs composing these are the same ones that are selected by function codes 8 - 11.

C18 – RAM block 1 (256 points maximum)
C19 – RAM blocks 1 & 2 (512 points maximum)
C20 – RAM blocks 1, 2 & 3 (768 points maximum)
C21 – RAM blocks 1, 2, 3 & 4 (1024 points maximum)

Note that a set of joined together RAM blocks may not be programmed as a unit. Each block must first be separately selected (with function codes 8 - 11) and programmed. The start and stop addresses, if selected, will be applicable to each block of stacked PROMs or RAMs.

20. **Memory Address (X)** – Gives data (Y) value at the address (X) queried.

Example: X125 33Y – At address 125 in the 0 - 255 address block, the data value is 33 in a 0 ±127 range.

This parameter is used to select the address of the data point in the waveform memory which is read and programmed by the memory data (Y) parameter. This parameter also sets the cursor register (immediately, without Execute). This register is used to cause a pulse to occur on the rear panel CURSOR OUT BNC connector whenever the data point in the waveform memory at the address stored in the cursor register is being output.

This key has an automatic increment feature. If pressed (or "X" is programmed over the GPIB) twice without pressing any other key, then the second pressing will increment the memory address and display it and the data at the new address. Additional pressings will continue to increment until the sequence is broken by pressing another key. Holding the key down will continuously increment to the next address and show the corresponding data.

21. **Memory, Data (Y)** – Provides access to the waveform memory data point located at the address specified by the memory address parameter (X) in the memory block specified by the function parameter (C).

Example: Y33 – At last address (X) queried in the 0 - 255 address block, the data value is 33 in a 0 ±127 range.

This key has an automatic increment feature. If pressed (or "Y" is programmed over the GPIB) twice without pressing any other alpha key, then the second pressing will increment the memory address parameter (X) value and display the Y data at the next address. Additional pressings will continue to increment the address until the sequence is broken by pressing another alpha key. Holding the key down will continuously increment the address and data displayed.

Refer to paragraph 3-7 for operation.

22. **Output, Off or On (P)** – Shows connection or no connection between the output amplifier and the BNC connector. This parameter makes the connection by a relay.

P0 – Output to ARB OUT (ATTEN) BNC disconnected (*I/C*)
P1 – Output to ARB OUT (ATTEN) BNC connected

23. **Output, Amplitude (A)** – Shows status.

Example: A3.25V – The output voltage is 3.25V p-p into 50Ω in a range of 1 to 10V p-p. A1 (*I/C*)

Refer to paragraph 3.13 for operation.

24. **Output, Offset (D)** – Shows status.

Example: D2.05V – Output dc offset is 2.05V into 50Ω in a range of 0 ±5.00V. D0 (*I/C*)

Refer to paragraph 3.13 for operation.

25. **Smoothing, Off or On (O)** – Shows status:

O0 – Smoothing off (*I/C*)

O1 – Steps of data making up the waveform are smoothed for a more continuous waveform.

Refer to paragraph 3.8 for operation.

26. **Manual, Hold (H)** – In triggered mode (B1), pressing the key stops and holds the output at the instantaneous value. The address stopped on is shown on the readout. Trigger (J) the generator to continue output waveform. Refer to paragraph 3.15 for hold use.

Example: H102 – Holding at address 102.

27. **Manual, Trigger (J)** – Triggers the output when in trigger mode. Refer to item 13 and paragraph 3.15 for trigger use.

28. **Exponent (E)** – Consider this key (E) as part of the numbered key group. The value keyed after E is the exponent of a X 10 multiplier.

Example: E6 = $X\ 10^6$

29. **Clear Entry** – Erases an incomplete numeric entry (indicated by a display with an asterisk on the right-hand side). The display is replaced by the previous value of the parameter that was being reprogrammed. This key is used to clear out a programming entry in case an incorrect key was pressed, or if the user changes his mind and decides not to change the parameter value. This key has no effect if there is no incomplete entry in progress (no asterisk on the right-hand side).

30. **Execute (I)** – This key causes an execute cycle which transfers from the display memory to the waveform generator circuits the values of the following parameters:

Internal or External Clock (N)
Sample Time (T)/Block Rate (F)
Preset or Monitor Trigger Mode (M)
Preset Length of Burst (L)
Full or Partial Block (U)
Start Address (V)
Stop Address (W)
Function (C)
Output On or Off (P)
Amplitude (A)
Offset (D)
Smoothing On or Off (O)

Causing an execute cycle is the only way to update these parameters in the waveform generator circuits. An execute cycle also restores a ramp to zero (G) to the prior status. Note that the waveform memory data (Y) and cursor register (X) do not require an execute cycle; when either of them is programmed with a new value, that value is sent immediately to the waveform circuits.

31. **Plus and Minus** – Changes the sign on the displayed number. If the sign change is made after the exponent (E) is programmed, the sign change affects the exponent only.

Example: –1.25E–2 = 1.25–E–2 = –1.25E2– = –0.0125 = -1.25×10^{-2}.

3.3 POWER

Power is turned on and off with a front panel pushbutton. When power is turned on, wait approximately two seconds before programming. When the power is turned on, the Arb is ready to accept commands. At least two seconds must elapse between power off and power on for proper reinitialization of logic. When the power comes on, the Arb output is automatically disconnected to allow loading of a program; line transients on the output are avoided. The Arb must get an execute command to provide an output.

3.4 INPUTS AND OUTPUTS

Refer to figure 2-1 for connector locations.

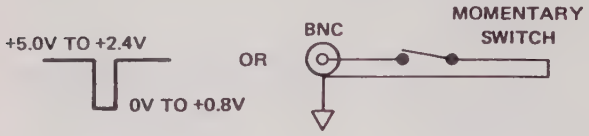
CURSOR OUT TTL Output – This output is a positive going TTL pulse coincident and of the same width with each output of a particular data point. The data point is designated by storing its memory address in the cursor register. Refer to paragraph 3.2.2, item 20.

SYNC OUT TTL Output – This output is a positive going TTL pulse whose leading edge is coincident with each stop address of a waveform and whose trailing edge is coincident with each start address of a waveform being output. In full block operation this pulse rises at address 255 and falls at address 0. During trigger mode the pulse rises and remains up until the Arb is triggered, which is coincident with the start address. The pulse normally appears at the end of each cycle and stays up after the last cycle of the triggered burst.

ARB OUT (HI) 0Ω Output – This output is a $< 1\Omega$ source of the generated waveforms. This BNC output is directly connected to the output amplifier.

ARB OUT (ATTEN) 50Ω Output – This output is a 50Ω source of the generated waveforms. The connnection of the BNC output with the amplifier output is program or front panel controlled via a relay.

The ramp to zero, external hold and external trigger BNC input connectors accept either a TTL low going pulse or momentary switch closure:



RAMP TO ZERO TTL Input – When this connector is pulsed, the waveform at the ARB OUT connectors is instantaneously held at its voltage level and ramped to 0 volts in approximately 15 seconds.

EXT HOLD TTL Input – When the Arb is operating in a trigger mode and this connector is pulsed, the waveform at the ARB OUT connectors is instantaneously (asynchronously to the reference clock) held at its voltage level. Use a manual, GPIB or rear panel applied trigger to continue operation. Refer to paragraph 3.15 for trigger and hold use.

EXT TRIG TTL Input – When the Arb is operating in a trigger mode and this connector is pulsed the output dictated by the trigger mode setting is initiated. Refer to paragraph 3.15 for triggered hold use.

EXT REF TTL Input – This input is used when the Arb is set to operate with an external clock reference. For proper operation, use a TTL signal of dc to 11 MHz, if the Arb is set to continuous mode or 500 kHz to 11 MHz, if set to trigger mode. The ratio of the external clock frequency to 10 MHz (standard internal clock) is a factor used in determining specific output frequencies.

REF OUT TTL Output – This connector is a TTL source at the reference clock frequency.

3.5 BASIC COMMAND STRUCTURE

The Arb is programmed by sending ASCII coded characters (refer to Appendix A) to the microprocessor via keyboard or GPIB (figure 3-3). If input characters are present on more than one input port, they are read first from the GPIB and last from the keyboard. Thus, if the GPIB is continuously supplied with characters, then no characters will ever be read from the keyboard.

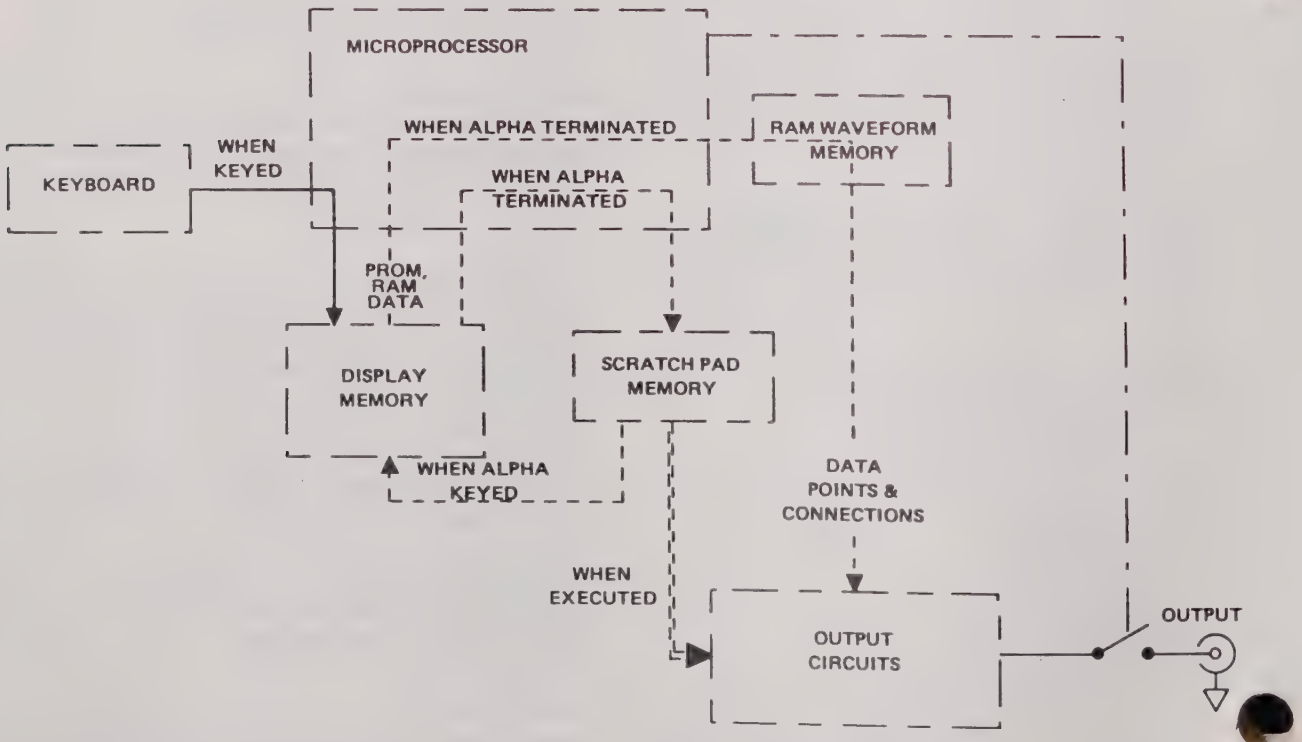


Figure 3-3. Command and Memory Structure

Characters used to program the Arb are divided into classes:

1. Alphabetic Characters — The characters A thru Z, except E (characters on lower left of front panel keys).

2. Numeric Characters — The characters 0 thru 9, E, —, decimal point (.).

3. Terminator Character — Initially the ASCII line feed character (LF). This can be changed by programming.

4. Nonprogramming Characters — Any character not in one of the above classes.

The alphabetic characters are used to select *actions* or parameters. An action is a sequence of events which happens immediately when the character which selects it is read by the microprocessor. A parameter is a number value which may be changed by programming.

To program an action, simply program the proper alphabetic character from either input port. The action will then take place, but only if the instrument is in the *enabled* state at the moment when that character is read by the microprocessor. Enabled states are:

Input Port	Arb Condition
Keyboard	GPIB not in Remote
GPIB	GPIB in Remote

Refer to REN, paragraph 3.16.1 for selection.

To examine the current display value of a parameter, simply program the proper alphabetic character from either input port. The current value will then be displayed on the front panel. This occurs whether or not the instrument is enabled. If the character programmed does not correspond to a legal setting in the instrument, nothing happens.

The numeric characters are used to program new parameter values. To change a parameter value, first program the alphabetic character which selects the parameter (F = frequency, etc.). The instrument must be enabled at this time, or it will not allow the new value to be entered. Next, program the new value using numeric characters; the instrument must be enabled for these as well. Any sequence of characters (called the argument of the parameter) which gives the new value is acceptable. For example, all of the sequences in table 3-2 will cause the value 100 to be programmed.

The number to the left of the "E" is the mantissa; the number to the right (one or two digits allowed) is the exponent.

Table 3-2. Examples of Value Programming

ASCII	Keyboard	Std Notation
100	100	100
0100	0100	100 (leading zeros are ignored)
1E2	1 EXP 2	1×10^2
.01E4	.01 EXP 4	$.01 \times 10^4$
.01E34	.01 EXP 34	$.01 \times 10^4$ (last exponent digit only is used)
1000E-1	1000 EXP +/– 1	1000×10^{-1}
1E-2-	1 EXP +/– 2 +/–	1×10^2 (two minus signs cancel)
1E.2	1 EXP .2	1×10^2 (decimal points in exponent are ignored)

The resulting value is the mantissa times 10 to the exponent power. Only one decimal point and one "E" (keyboard EXP) are allowed per number; additional ones are ignored. The sign toggle character may appear any number of times. It causes the sign of the mantissa (if "E" has not been programmed) or the exponent (if "E" has been programmed) to be reversed (if negative, then positive, and vice versa) each time it appears. Any number of nonprogramming characters may be interspersed with the numeric characters, as they have no effect. If an undesired value is entered, the clear entry key can be used to erase it.

Several parameters require codes for specific selections; for example, the function codes of 0 thru 11 to select sine, triangle or square waves, etc. Refer to paragraph 3.2.2 for parameter codes.

Since the number input format is so general, the microprocessor must be told when the last numeric character has been entered so it can evaluate the number. This is done by programming either an alphabetic or terminator character. When this is done, the new value is first tested to see if it is a legal value for the setting being changed. If it is not legal, an error message is displayed on the front panel and the setting value in the display memory is not changed. If it is legal, the new value is entered into the display memory; however, it is not sent to the output circuits.* That can be done only by programming the "I" action (EXEC key on the front panel). When a new value is entered into the instrument memory, it is rounded to the number of significant digits specified by the parameter being changed, as specified by table 3-3.

Table 3-3. Round Offs

Letter	Parameter Name	Number of Digits
A	Amplitude	3
O	Offset	3
F	Block Rate	Not rounded
T	Sample Time	4**
All other settings		Nearest integer

*Exceptions: When a RAM waveform value (Y) is programmed, the value is sent immediately to the RAM memory and thus alters the output waveform without use of execute. Also, when a memory address (X) is programmed, the value in the cursor register is updated, thus changing the time when the CURSOR OUT pulse appears.

** Refer to paragraph 3.9.

3.6 COUNTER GENERATED WAVEFORMS

The counter generated waveforms, square, triangle and ramp (figure 3-4) are simply called up by function selection (paragraph 3.2.1, item 19). Their characteristics which are due to digital generation are discussed in section 4.

3.7 MEMORY DATA (Y) FOR ARBITRARY WAVEFORMS

This parameter is used to read and program data points in the waveform memory. The MEMORY DATA key provides access to the data point located at the address specified by the memory address parameter (X) in the memory block specified by the function parameter (C). Programming a value into this parameter changes the data point value if the memory block is a RAM block; otherwise, nothing happens. *This change occurs immediately without use of an execute.* This parameter has an automatic increment feature. If the memory data key (Y) is pressed (or Y is programmed over the GPIB) twice without pressing any other alpha key, then the second pressing will increment the memory address parameter (X) value and display the Y data at the new address. Additional pressings will continue to increment the address until the sequence is broken by pressing another alpha key. Note that it is possible to program a new Y value between pressings of the memory data key; this provides a convenient way to program successive data points using only the memory data key. For example, a ramp from 127 to −127 can be programmed as follows: Y127Y126Y125Y . . . . . Y−126Y−127Y−127 (a total of 256 settings). This parameter also provides an alternate "interpolation mode" form of programming used to draw straight line segments. This mode is activated when two pairs of X,Y data point settings are programmed with no other keys pressed (or no other alphabetic characters programmed over the GPIB). After the second pair is programmed, a line is drawn between the first and second points, approximating a straight line as closely as possible.* Additional X,Y pairs may be programmed and lines will then be drawn between the second and third, third and fourth, etc., points. To exit from interpolation mode, just press a key other than memory address or memory data. Table 3-1, step 8, shows an example of programming a complete block of RAM using the interpolation mode.

Important notes for the interpolation mode are:

1. Each parameter (X or Y) of the X,Y pairs must be programmed with a new value. Just pressing a memory address or data key is not sufficient.

2. The parameters must be entered in the order XYXY . . . (not YXYX).

3. No other alpha keys may be pressed during an XYXY . . . interpolation sequence.

   Example: X0Y0X100Y100I will draw a straight line from (0,0) to (100,100), but X0Y0AX100Y100 will only set the data points at memory locations 0 and 100 to 0 and 100, respectively, leaving the other 254 data points untouched.

3.8 SMOOTHING (O)

This parameter selects whether waveform smoothing is disabled (O0) or enabled (O1). If smoothing is enabled, and the sample time is 20 μs or longer, then 100 finely spaced data points are inserted on a straight line between every pair of data points as shown in figure 3-5. There is an exception: No smoothing is done between data points whose Y values differ by more than 63. For the effect of smoothing on sample time round off, refer to paragraph 3.9.

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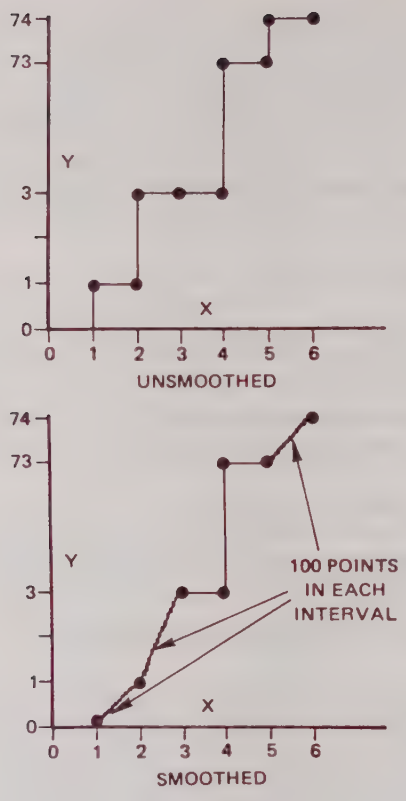
*When composing waveforms by entering data only when a change in slope is required, the microprocessor automatically draws the line (step linearly) between the points entered. If the slope

$$\frac{\text{Change in Y}}{\text{Change in X}}$$

is not a whole number, the microprocessor plots two or more line segments that approximate a single line segment as nearly as possible. ("Line segment" referred to here is a set of linear steps.)



NOTE

No smoothing during the time slot 4 to 5, because the data point values at X = 4 (3) and X = 5 (73) differ by more than 63. Smoothing does occur at all other times (0 to 4 and 5 to 6).

Figure 3-5. Waveform Smoothing

3.9 SAMPLE TIME (T) AND WAVEFORM SMOOTHING

Hardware dictates a stepping time resolution of 100 ns. This results in sample time round off, as shown in table 3-5. Sample time round off is also affected by waveform smoothing. Waveforms can be smoothed by incrementing between data points with 100 steps for each original step (with the exception of steps with greater than 63 point change which are not smoothed).

Both sample time steps and smoothing steps are clock controlled; PROM and counter waveforms have a minimum step time of 200 ns while RAM waveforms have a minimum step time of 500 ns. Arb software detects sample times of less than 200 ns and gives an ERROR readout when an attempt is made to place those times in scratch pad memory. Notice, then, that RAM waveforms may be programmed and output at faster sample times (200 through 700 ns) than specified. Waveform deterioration will result when this is done.

When smoothing is programmed (100 smoothing steps per sample time), smoothing cannot occur unless *sample time* is 100 times greater than the 200 ns stepping time minimum; i.e., 20 μs.

When the sample time is programmed, the unrounded value is retained. Rounding is done when the execute action takes place, allowing the precision of the programmed value to be the maximum possible. For example, assume that the sample time is programmed to be 23.45 μs with smoothing off. In this case, the sample time will be rounded to 3 digits (23.5 μs) when execute occurs. If smoothing is then turned on, rounding will be to one digit (20 μs) when execute occurs. If smoothing is subsequently turned off again, rounding will once more be to 3 digits, and the value programmed into the waveform generation circuits at execute time will again be 23.5 μs. When this parameter is displayed on the front panel, it is shown rounded to the proper number of digits.

3.10 CLOCK TIME UNITS (S)

This parameter selects whether the sample time parameter (T) is programmed and displayed in seconds, minutes or hours. However, since the Arb waveform generator circuits are programmed in seconds, sample times programmed in minutes or hours must be converted to seconds by the microprocessor. This may result in sample times which are not exactly equal to the programmed value. For example, 6.789 minutes is 407.34 seconds, which requires 5 digits of programming accuracy. Since the Arb has only 4 digits, the value programmed is 407.3 seconds, or 6.788333 minutes. The actual time programmed will be displayed when sample time (T) is selected.

3.11 FULL OR PARTIAL BLOCK (U)

The full or partial block parameter selects whether a block consists of either the entire 256 points available or a portion of them selected by the block start address (V) and block stop address (W) parameters. If a full block (U0) is selected, the waveform is output by sequentially reading the sample points from the selected block starting at address 0 and ending at address 255. If a partial block (U1) is selected, the sample points are sequentially read starting at the block start address parameter value and ending at the block stop address parameter value. The start and stop address parameters should not be set to the same value if a partial block is selected, because no waveform will be generated. If an execute (I) is done in this case, an ERROR will be displayed, although the start and stop addresses will be programmed into the waveform generator circuits anyway. If two or more blocks are joined together (see item 19) and partial block (U1) is selected, then the resulting waveform is composed of the selected portion of *each* block. The start ad-

dress may be greater than the stop address; in this case, the block "wraps around" from address 255 to address 0.

Table 3-5. Sample Time Round Off

Sample Time	No. of Significant Digits	
	Smoothing Off	Smoothing On
200 to 900 ns*	1	1**
1 to 9.9 μs	2	2**
10 to 19.9 μs	3	3**
20 to 99.99 μs	3	1
100 to 999.9 μs	4	2
1 to 9.999 ms	4	3
10 ms or longer	4	4

*RAM waveforms are not spec'd for sample time of:

Smoothing off: 200 - 400 ns

**Even if smoothing is programmed, no smoothing occurs for sample times shorter than 20 μs.

3.12 BLOCK RATE (F)

The block rate parameter is not a separate parameter. Instead, it is an alternative means of setting the sample time parameter in terms of the repetition frequency of blocks. When a block rate is programmed, the sample time necessary to produce it is computed from the number of blocks stacked together; the programmed block rate and the current size of a block as selected by full/partial block parameter and the start and stop block address parameters.

NOTE

When partial block is selected, the block rate is the rate of the partial block.

It is not possible, in general, to compute a sample time which will produce the desired frequency exactly. Consequently, when the block rate is displayed on the front panel, the number displayed is not the block rate that was programmed, but the block rate actually being produced.

If the full/partial block parameter code is zero,

$$\text{Sample Time} = \frac{1}{\text{Block Rate} \cdot 256 \cdot \text{No. of Blocks}}$$

If the full/partial block parameter code is one and the stop address is greater than the start address,

$$\text{Sample Time} = \frac{1}{\text{Block Rate} \cdot (\text{Stop Adr} - \text{Start Adr} + 1) \cdot \text{No. of Blocks}}$$

If the full/partial block parameter code is one and the stop address is less than the start address,

$$\text{Sample Time} = \frac{1}{\text{Block Rate (Stop Adr} - \text{Start Adr} + 257) \cdot \text{No. of Blocks}}$$

3.13 AMPLITUDE (A) AND OFFSET (D)

The amplitude parameter selects the amplitude generated by a waveform memory data point value of +127 (or the negative amplitude generated by a value of −127) at the ARB OUT (ATTEN) BNC connector. Smaller data point values will produce proportionately smaller amplitudes. Values from 1 mV p-p to 10V p-p (and −1 mV p-p to −10V p-p) into 50Ω and 0 may be programmed with 3 digit resolution. Negative values of amplitude invert the waveform.

The offset parameter selects a dc offset to be added to the output waveform. Values from 1 mV to 5V (and −1 mV to −5V) and 0 may be programmed with 3 digit accuracy into 50Ω.

The amplitude and offset are not completely independent of one another, because they share a common output amplifier and attenuator (see figure 3-5). In certain cases it may become necessary to decrease the number of digits of resolution of amplitude or offset (or both) in order to either prevent clipping in the output amplifier or to make the programmed value of offset (or amplitude) appear at the output despite an unfavorable attenuator setting required by a larger value of amplitude (or offset). The sum of amplitude or offset controls the output amplifier and attenuator. The output amplifier is limited to 10V p-p (into 50Ω). The attenuator operates at one of the values of $X\ 10^{0}$, $X\ 10^{-1}$, $X\ 10^{-2}$ or 10^{-3} (0 dB, −20 dB, −40 dB, −60 dB).

If the absolute peak value at the amplifier input (which is the sum of the absolute values of the amplitude and offset mantissas, when amplitude and offset are expressed in scientific notation) exceeds 10V, then logic divides the values

programmed into the amplitude and offset by 10 and, to maintain the desired output level, decreases attenuation by a factor of 10 also. If this must be done, then one digit of resolution is lost from both amplitude and offset. This adjustment cannot be done if the sum of the absolute values of the programmed amplitude and offset (which is the X 10 multipliers as well as the mantissas) is greater than 10V; in this case, the output will be clipped.

To determine if there is clipping or loss of resolution, perform the following calculations.

1. Add twice the absolute value of the desired offset to the absolute value of the desired amplitude. If the sum exceeds 10, clipping will occur. If not, go to step 2 to determine a trial attenuator setting.

2. Write the larger of the absolute amplitude or twice absolute offset in the form N.NN X 10^X, where N.NN is between 1.00 and 9.99. Then X 10^X is the trial attenuator setting. Perform step 3 to determine if the amplifier output would be clipped for the trial attenuator setting.

3. Take the sum of amplitude and offset computed in step 1 and write it in the form MM.MM X 10^X, where x is the exponent computed in step 2. If MM.MM is greater than 9.99, then one digit of resolution must be lost from both amplitude and offset in order to prevent the output amplifier from clipping.. Perform step 4 if there was no loss of resolution to determine if the smallest amplifier input caused too many significant digits.

4. Write the amplitude or twice the offset, whichever is smaller in absolute value, in the form Y.YYZZZ X 10^X, where x is the exponent computed in step 2. If any of the digits ZZZ are not zero, then resolution is lost, because only Y.YY can be used to program the waveform generator circuits.

Example A

Ampl = –3.43
Offset = 2.33

Step 1. 4.66 + 3.43 = 8.09. There is no clipping.
Step 2. Twice absolute offset is larger. 4.66 = 4.66 X 10^0. Therefore, x = 0.
Step 3. 5.97 = 5.97 X 10^0. Therefore, there is no loss of resolution in either parameter.
Step 4. Absolute amplitude is smaller. –3.43 = –3.43000 X 10^0. ZZZ = 000 and there is no loss of resolution anywhere.

Example B

Ampl = 0.0456
Offset = 0.0393

Step 1. 0.0786 + 0.0456 = 0.1242. There is no clipping.
Step 2. 0.0786 = 7.86 X 10^{-2}. X = –2.
Step 3. 0.1245 = 12.45 X 10^{-2}. Since 12.45 exceeds 9.99, there is a loss of one digit of resolution in both amplitude and offset. This means that the offset will be 0.039 (not 0.0393) and the amplitude will be 0.045 (not 0.0456).
Step 4. Not required.

Example C

Ampl = 2.58
Offset = 0.123

Step 1. 0.246 + 2.58 = 2.826. There is no clipping.
Step 2. Absolute amplitude is larger. x = 0.
Step 3. 2.703 = 2.703 X 10^0. No loss of resolution so far.
Step 4. Absolute offset is smaller. 0.246 = 0.24600 X 10^0. Y.YY = 0.24 and ZZZ = 600. Therefore, one digit is lost in the offset value, which will be 0.120, not 0.123.

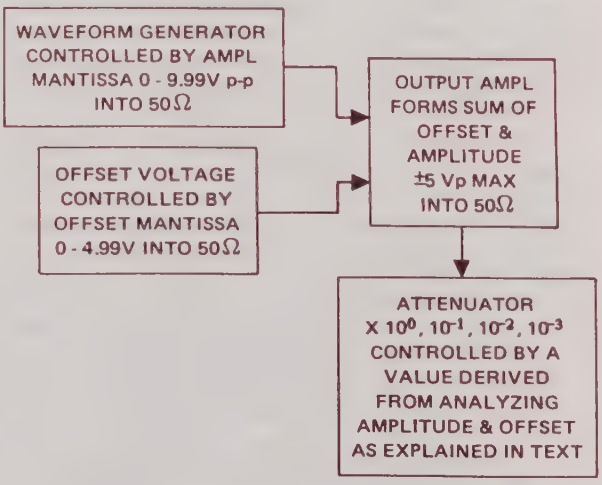

WAVEFORM GENERATOR CONTROLLED BY AMPL MANTISSA 0 - 9.99V p-p INTO 50Ω
OFFSET VOLTAGE CONTROLLED BY OFFSET MANTISSA 0 - 4.99V INTO 50Ω
OUTPUT AMPL FORMS SUM OF OFFSET & AMPLITUDE ±5 Vp MAX INTO 50Ω
ATTENUATOR X 10^0, 10^{-1}, 10^{-2}, 10^{-3} CONTROLLED BY A VALUE DERIVED FROM ANALYZING AMPLITUDE & OFFSET AS EXPLAINED IN TEXT

Figure 3-5. Hardware Diagram of Amplitude and Offset Generation

3.14 ERRORS

Programmed values are evaluated by the microprocessor when it receives a following alpha or terminator character. This character acts as a terminator, indicating that the operator is through selecting the numerical value. If, after round off, the value is out of range for the selected parameter, an

ERROR message is placed on the display and the scratch pad memory is not changed. If executed, output would be the current values in scratch pad memory.

When the execute key is pressed, two error tests are made: one for clipping (absolute value of amplitude plus absolute value of offset greater than 10V p-p into 50Ω) and one for misprogramming of the block start and stop addresses (start (V) and stop (W) addresses equal and partial block mode enabled (U1)). If clipping error is detected, ERROR will be displayed on the front panel and the incorrect parameters will be sent unaltered to the waveform circuits. If start and stop addresses are equal, ERROR is displayed and the last legal addresses are retained.

3.15 PRESET AND MONITOR TRIGGER (M)

In both modes the waveform may be stopped at any time with a hold command (H), and then resumed from the place where stopped with a trigger (J). If the preset mode is selected, the trigger will reset the cycle counter before resuming the waveform, thus restarting the process of generating a preset number of cycles. In this case, the preset length (L) parameter determines the number of cycles generated after the trigger, with the first cycle being composed of the remaining portion of the cycle that was interrupted by the hold command.

3.16 GPIB

The GPIB interface is an implementation of IEEE Standard 488-1975. It supports the following interface functions: Source Handshake (SH1), Acceptor Handshake (AH1), Talker (T6), Listener (L4), Service Request (SR1), Remote Local (RL2), Device Clear (DC1) and Device Trigger (DT1).

Devices connected to the GPIB can have one or more of the three capabilities: talk, listen and control. The talk capability allows a device to send data (such as voltmeter or counter readings) out over the bus. The listen capability allows a device to receive data (such as device programming information or a printer receiving data to be printed) from the bus. The control capability allows a device to control the flow of data over the bus. Although there may be more than one device connected to the GPIB with control capability, only one device at a time may exercise that capability on the bus. One device's control capability must be active at all times; this device is called the controller.

Programming examples are given in Appendex B.

NOTE

When ATN goes true, the GPIB interface will go from the AIDS state to the ACRS state in less than 200 nanoseconds and will ignore the status of the DAV signal, in accordance with the IEEE 488-1975 specifications. This action may create problems for controllers that try to Take Control Synchronously (TCS).*

**Refer to AH state diagram and C state diagram of the IEEE 488-1975 standard.*

3.16.1 Bus Lines Defined

The GPIB consists of 16 signal lines, as shown in table 3-6. Their functions are:

DIO1 - DIO8	These eight lines (Data In/Out) are used to send commands and data encoded as 8-bit binary numbers (bytes).
ATN	This line (Attention) is operated only by the controller. It specifies whether the information on lines DIO1 - DIO8 is data (false) or a command (true). Whenever ATN is set true, no activity is allowed on the bus except for controller-originated messages; additionally, every device connected to the bus is required to receive and process every command sent by the controller.
DAV, NRFD, NDAC	These are the "handshake" lines (Data Valid, Ready For Data and Data Accepted) which regulate the transmission of information over the lines DIO1 - DIO8. For each command or data byte transferred, a complete handshake cycle must occur. This handshake is designed to hold up the bus until the slowest device has accepted the information.
EOI	When ATN is false, this line (End Or Identify) indicates that the data on lines DIO1 - DIO8 is (true) or is not (false) the last byte of a data message. Refer to paragraph 3.16.4 for terminator character identification.
REN	This line (Remote Enable) is used to control whether devices on the GPIB are in local or remote mode. In local mode, devices respond to front panel commands and do not respond to GPIB-originated commands. In remote mode the situation is reversed: GPIB-originated commands are obeyed while front panel commands are ignored. A device enters the remote state whenever it receives its listen address (refer to para-

graph 3.16.2, GPIB Commands) at the same time as REN is in the remote state. The device then stays in the remote mode until either the REN line is put in the local state or the device receives a Go-To-Local (GTL) command.

SRQ — This line (Service Request) is used by the devices on the bus to signal the controller that they need attention. (Refer to paragraph 3.2.2, item 3, for Service Request Enable.) Since the SRQ line is common to all devices, additional tests must be made to determine which devices are signaling. The Serial Poll capability is usually employed to accomplish this.

IFC — This line (Interface Clear) is used by the controller to reset the interface logic in all devices connected to the bus to a known initial state.

Table 3-6. GPIB Lines and Commands

Bus Lines	
DIO1 - DIO8	Data In/Out Lines
ATN	Attention
DAV	Data Available
NRFD	Ready For Data
NDAC	Data Accepted
EOI	End Or Identify
REN	Remote Enable
SRQ	Service Request
IFC	Interface Clear

GPIB Commands	
Listen Address	
Talk Address	
Secondary Address	
Universal Commands	
DCL	Device Clear
SPE	Serial Poll Enable
SPD	Serial Poll Disable
Addressed Commands	
GTL	Go To Local
SDC	Selective Device Clear
GET	Group Executive Trigger

3.16.2 GPIB Commands

Commands are sent over lines DIO1 - DIO8 with ATN true. They are divided into five classes.

3.16.2.1 Listen Addresses

Listen addresses are used to command a device to read any data bytes transmitted over lines DIO1 - DIO8. There are 31 different available addresses (hexadecimal codes 20 thru 3E, ASCII codes "SP" thru ">"). A thirty-second address, called unlisten (hexadecimal 3F, ASCII "?"), is used to command all devices not to read data bytes. The Arb's listen address is selected by the rear panel DIP switch, which specifies the lower 5 bits of the address. (Refer to table 2-2.)

3.16.2.2 Talk Addresses

Talk addresses are used to command a device to transmit data over lines DIO1 - DIO8 whenever ATN is false. There are 31 different available addresses (hexadecimal codes 40 thru 5E, ASCII codes "@" thru "↑"). A thirty-second address, called untalk (hexadecimal 5F, ASCII "→") is used to command all devices to cease talking. The lower 5 bits of the Arb's talk address are selected by the same rear panel DIP switch used to select the listen address. Thus, if the Arb's listen address is hexadecimal 21 (ASCII "!"), the talk address is hexadecimal 41 (ASCII "A").

3.16.2.3 Secondary Addresses

Secondary addresses are used following a talk or listen address to provide the ability to address more than the 31 devices provided for by simple talk or listen addresses. Secondary addresses are ignored by the Arb.

3.16.2.4 Universal Commands

Universal commands are used to command a device to perform designated actions. Universal commands are recognized at all times. Universal commands performed by the Arb are:

a. **Device Clear (DCL).** Resets the following parameters to the power on state.

Amplitude	1 volt
Offset	0 volts
Mode	Continuous
Function	Sine
Output	Off
Clock Int/Ext	Internal
Time Unit	Seconds
Sample Time	20 μs
Preset/Monitor	Preset
Preset Length	1
Full/Part	Full
Start Address	0
Stop Address	255
Memory Address	0
Smoothing	Off

This information is also set into the waveform generating circuitry. The data in the waveform memory RAMs are not affected.

b. **Serial Poll Enable (SPE).** Causes the instrument to engage in a serial poll by responding with the serial poll status byte when addressed as a talker. Bit 7 of this byte will be on, if service is being requested on the SRQ line. When the status byte is read, it is reset to zero, and the SRQ line is released (of course, it may still be held down by other devices). The status byte is also available by reading the Arb's talk message number 2. When this message is read, the status byte is reset to 0 and SRQ released as for the serial poll.

c. **Serial Poll Disable (SPD).** Removes the instrument from the serial poll mode activated by the SPE command.

3.16.2.5 Addressed Commands

Addressed commands are used to command a device to perform designated actions. Addressed commands are recognized only when the instrument is addressed as a listener. Addressed commands performed by the Arb are:

a. **Go To Local (GTL).** Commands the Arb to go to the local mode (see explanation for REN line, paragraph 3.16.1).

b. **Selective Device Clear (SDC).** Same action as for Device Clear (DCL) command, paragraph 3.16.2.4.

c. **Group Execute Trigger (GET).** This command transfers the programmed waveform values to the waveform generation circuits, and then sends a trigger pulse. This is the same sequence of events that would happen if an execute, then a trigger action were processing a previously sent programming string), this command is completed within a few milliseconds of being received; otherwise, it is not done until the program string is completely processed to ensure that up-to-date values are sent to the instrument circuits.

3.16.3 GPIB Data Transfers

The Arb will both accept programming characters and transmit status information over the bus. To program the instrument, first send the listen address (with ATN on), followed by the programming data (in ASCII, with ATN off). The instrument microprocessor accepts the data as fast as possible, until either 40 characters are received or there is a pause during the transfer of data. At that time, the entire string of received characters is scanned by the microprocessor, which carries out the programming instructions contained in it. While this is happening, the instrument can accept an additional 40 characters of data over the bus; if more are sent, the bus will hang until the microprocessor completes a scan and accepts the next 40 character string. If the EOI line is asserted while sending a character to the Arb, the currently programmed terminator character will be put into the input string following the character with the EOI.

To read a message from the Arb, first send the talk address (with ATN on) over the bus. The instrument will then send the message currently selected by the talk message select (R) parameter. The last character of this message will be the currently programmed terminator character with the EOI line asserted.

3.16.4 GPIB Talk Message and Terminator Character (R)

One key (or "R" on GPIB) controls two parameters: the terminator character and the type of talk message sent when the Arb is addressed to talk over the GPIB. The terminator character is selected by programming a minus and the decimal value of the ASCII character that is to be the new terminator. Any ASCII character is acceptable except NUL (decimal code 0), so allowed values for programming the terminator range from −1 to −127. The terminator character has two uses. During output from the Arb over the GPIB, it is appended to every talk response. During input, it signals the end of a group of programming characters; in particular, it indicates the end of a number. At power on time, the terminator character is the line feed control character, decimal code 10. When the Arb sends a talk message, the terminator character is the last byte sent. In addition, the End Or Identify (EOI) line is pulled low (GPIB END message) during the terminator character transmission. If the device receiving the talk message requires a terminating character, but does not recognize either the line feed character or the END message, then a new terminator character must be programmed. For example, to change the terminator character to a carriage return (decimal code 13), program "R−13". Refer to Appendix A for ASCII codes.

The talk message parameter selects which of four messages will be sent when the Arb is addressed to talk over the GPIB. It is programmed with a positive integer code; allowed values are 0, 1, 2 and 3, with formats as follows:

R0 (*I/C*) State of Hold Status:
"H$_{\wedge}$0" if generator is not holding
"H$_{\wedge}$1" if generator is holding

R1 List of first nine errors since this message was last read. Each error is indicated by the GPIB programming letter of the parameter in which the error occurred.

Example: "E_A_B_F_A"
^ ^ ^ ^

The first letter, "E", indicates that this is an error response string. The other four letters indicate that an error occurred while setting first amplitude, then mode, then block rate, and again amplitude.

R2 This message gives the current value of the GPIB service request poll response, which describes why the Arb is asserting the SRQ line. This is the same byte that a GPIB controller would receive if it addressed the Arb and did a serial poll. If the SRQ line is being asserted by the Arb when this message is read, it is released.

Possible values are (the letter "P" indicates a poll message):

"P^^"	SRQ is not being asserted by Arb.
"P^E"	SRQ is asserted because of a programming error.
"P^H"	SRQ is asserted because the waveform generator went from a not-holding state to a holding state.
"P^M"	SRQ is asserted because both an error and a transition to holding occurred (conditions for "E" and "H" both true).

R3 This message gives the value currently associated with the parameter or status response selected by the last alphabetic character programmed to the Arb. If that character selects an action (such as execute or trigger), then the response is blank.

Examples (the letter V indicates a value of parameter message):

"V^A^6.5E—1"	response for amplitude = 650 mV.
"V^C^7"	response for function = PROM 3.
"V^I^"	response for execute (no numeric value returned).
"V^K^631"	response for monitor count (K) status showing a count of 631.
"V^H^49"	response for hold (H) action, showing address of sample point where held; hold is the only action which returns a numeric value.

The front panel display for this parameter shows the talk response code on the left and the decimal code (with a minus sign) for the terminator character on the right.

Example: R 0 −10

shows that the talk response code is zero and the terminator character is an ASCII line feed (whose decimal code is 10).

3.16.5 GPIB Service Request Enable (Q)

The key GPIB SRQ or the letter "Q" controls the conditions under which the Arb will make a service request (i.e., turn the SRQ line on). Note that programming this parameter does *not* change the state of the SRQ line. If SRQ is on, the only way to turn it off is to perform a serial poll or read talk message 2. If SRQ is off, the only way it can be turned on is by the occurrence of the condition(s) enabled by the SRQ enable parameter. Allowed values are 0, 1, 2 and 3, with the following effects.

Q0 SRQ disabled. The Arb will not turn SRQ on under any circumstances.

Q1 *(I/C).* SRQ enabled for programming errors. The Arb will turn SRQ on when a programming error is made from either the front panel or GPIB.

Q2 SRQ enabled for hold status coming on. The Arb will turn SRQ on when the waveform generator circuits go from a running to a holding state (refer to paragraph 3.15). Since the change is detected by the microprocessor, it may take as long as 10 ms between the transition to the holding state and the turning on of the SRQ (if a long block of data is being sent to the Arb via the GPIB, the maximum time increases to 20 ms).

Q3 SRQ enabled for both programming errors and hold status coming on. The Arb will turn SRQ on, if either a programming error (refer to explanation for Q1) or a transition to holding (refer to explanation for Q2) occurs. The status byte returned by a serial poll of the Arb will tell which condition turned SRQ on.

3.17 Input and Output Impedances

3.17.1 Arbitrary Waveform Outputs

The ARB OUT (ATTEN) connector is the main output and has a source impedance of 50Ω. Block amplitude in volts peak-to-peak and offset voltage in volts will be equal to programmed values when terminated into 50Ω.

The ARB OUT (HI) connector is an auxiliary output and has a source impedance of $<1\Omega$. Since this output does not pass throujgh the 50Ω attenuator and is not halved when terminated, it has a block amplitude in volts *peak* (not peak-to-peak) equal to the mantissa of amplitude and an offset in volts of *twice* the offset mantissa. Refer to paragraph 3.13 for amplitude and offset mantissas and exponents. This output should be terminated so that peak output current does not exceed 100 mA.

3.17.2 TTL Outputs

SYNC OUT, CURSOR OUT and REF OUT connectors have TTL level signals driven by standard TTL devices, capable of driving up to 10 TTL inputs or a resistive load of not less than 600Ω. In case of damage to these outputs by improper termination, the standard 7404 devices are socket mounted on the generator board for convenient replacement. U16D drives the REF OUT and CURSOR OUT and U10C drives the SYNC OUT.

3.17.3 TTL Inputs

The EXT TRIG, EXT HOLD, RAMP TO ZERO and EXT REF connectors accept external TTL level inputs. EXT REF presents a single, standard TTL load and is protected against inputs greater than +5V or less than 0V with discrete diodes. The other inputs also have diode protection, and respond to either TTL levels or momentary external contact closure between BNC conductor and shell. When a TTL signal is used, the low level input must sink 2.3 mA for the discrete pull-up resistor plus the standard TTL load of 1.6 mA, resulting in an input loading approximating 2½ loads.

3.17.4 Changing Source Impedance of the Main Output

The output impedance of the attenuated output [ARB OUT (ATTEN) 50Ω Rear Panel BNC, Figure 2-1] may be changed by removing the jumper on the generator board labeled ARB OUT (ATTEN) and inserting an appropriate 1W, 1% resistor, which will be in series with an existing 50Ω. For example, inserting a 550Ω resistor will give a 600Ω output impedance.

SECTION 4
CALIBRATION

4.1 INTRODUCTION

Periodic calibration will be required because of component aging, which depends upon instrument on-time and environment. Use three months as an initial calibration period. If possible, keep records of parameter values and increase the time between calibrations as the records indicate. Perform the procedure in table 4-1.

4.2 TEST EQUIPMENT

The following test equipment, or equivalent, is required for calibration.

Frequency Counter — 20 MHz, 0.01% accuracy, 5 digits
DVM — 0.05% accuracy, 3½ digits, 1 mV resolution
Oscilloscope . . . . . ≥30 MHz bandwidth

NOTE

The completion of the calibration procedure returns the instrument to correct alignment.

CALIBRATION LIMITS AND TOLERANCES ARE NOT INSTRUMENT SPECIFICATIONS

Instrument specifications are given in Section 1 of this manual.

Table 4-1. Calibration Procedures

NOTE: Where no horizontal line appears in a column, the entry for the previous step is still applicable. Unless otherwise specified, cal point and adjustments are on Arbgen board. No 50Ω load is used.

Step	Check	Tester	Cal Points	Program	Adjust	Desired Results	Remarks
1	Power Supply	DVM	R79	Power ON (or press RESET if already on) A10P1I	R26 (Pwr Sply Bd)	+15V ±20 mV	Allow ½ hour warm-up before checking.

NOTE: Slide the top cover back only to make adjustments; otherwise, keep the cover in place.

2	Reference Frequency	Frequency Counter	REF OUT BNC	C8T2E–6I	–	10 MHz ±.03% (3 kHz)	Disconnect cable at REF OUT after check.
3	Reference Voltage	DVM (set to read 5 Vdc)	TP13		R94 REF	+5 Vdc ±10 mV	See figure 4-1 for component locations.
4	Balance	DVM (set to 100 mVdc scale)	TP10		R107 AMPL BAL	< 5 mVdc	
5				O1I	R87 S/H BAL		

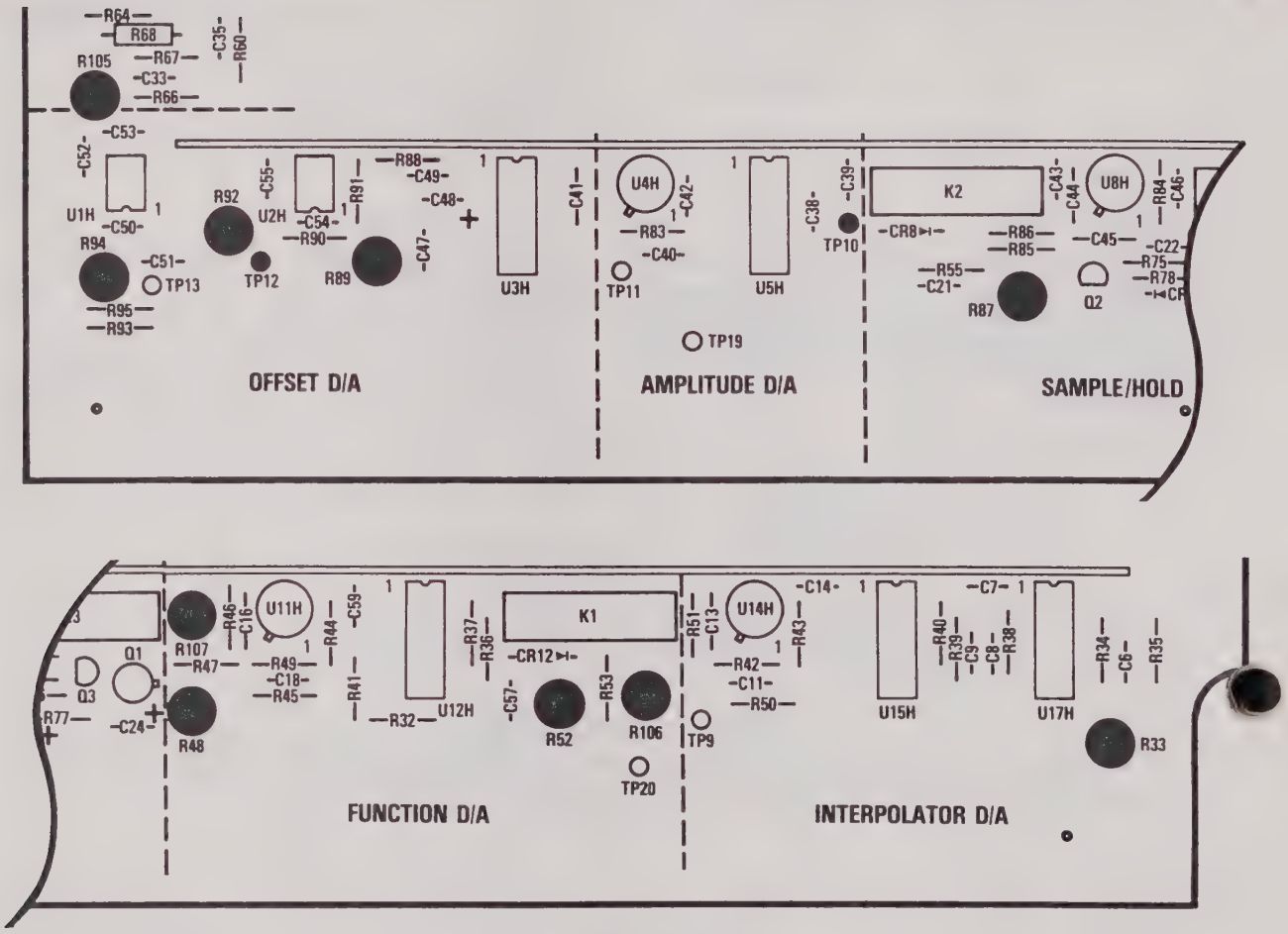


Figure 4-1. Component Location

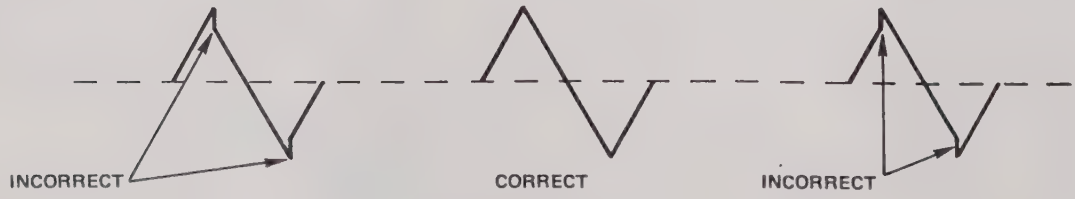


Figure 4-2. Proper Smoothing

Table 4-1. Calibration Procedures (Continued)

Step	Check	Tester	Cal Points	Program	Adjust	Desired Results	Remarks
6	Balance	Scope (10 mV/DIV)	ARB OUT (ATTEN) BNC	T2E–4I	R33 LO SMTH	Ccw until positive ramp appears, then cw until ramp just disappears	Connect SYNC OUT to scope external sync input.
7		DVM	TP10		R106 SMTH BAL	< 5 mVdc	
8	Offset		TP12		R92 OFST BAL	< 5 mVdc	
9			ARB OUT (HI) BNC		R105 PA BAL		
10		DVM (set to read 10 Vdc)		D5OOI	R89 OFST	10 Vdc ±20 mV	An ERROR warning is normal.
11		DVM		D–5I		See Remarks	If not –10 Vdc ±20 mV, remove ½ of the error with R89 and return to step 8.
12	Amplitude		ARB OUT (ATTEN)	D0C2T2E–2I	R48 AMPL	20V p-p ±20 mV	Check for < 50 mV offset. Offset = ½[(V+) + (V–)]
13	Program: T2E–4C9IX0Y0Y0Y1Y0Y2Y0Y4Y0Y8Y0Y16Y0Y32Y0Y63Y0Y64Y0X255Y0I. Set scope to observe an exponential train of positive pulses.						
14	Smoothing	Scope	ARB OUT (ATTEN)	O1I			Observe smoothing on all pulses except final pulse.
15					R33 LO SMTH	Proper smoothing cancellation. See figure 4-2.	Adjust scope to observe first few triangle waveforms.
16					R52 HI SMTH	Proper smoothing cancellation	Adjust scope to observe last few triangular waveforms.
	NOTE: If R33 was not adjusted in step 15, calibration is complete. Otherwise continue.						
17	Smoothing	DVM	TP10	C8I	R106 SMTH BAL	< 5 mV	
18				C9I			Return to step 15.

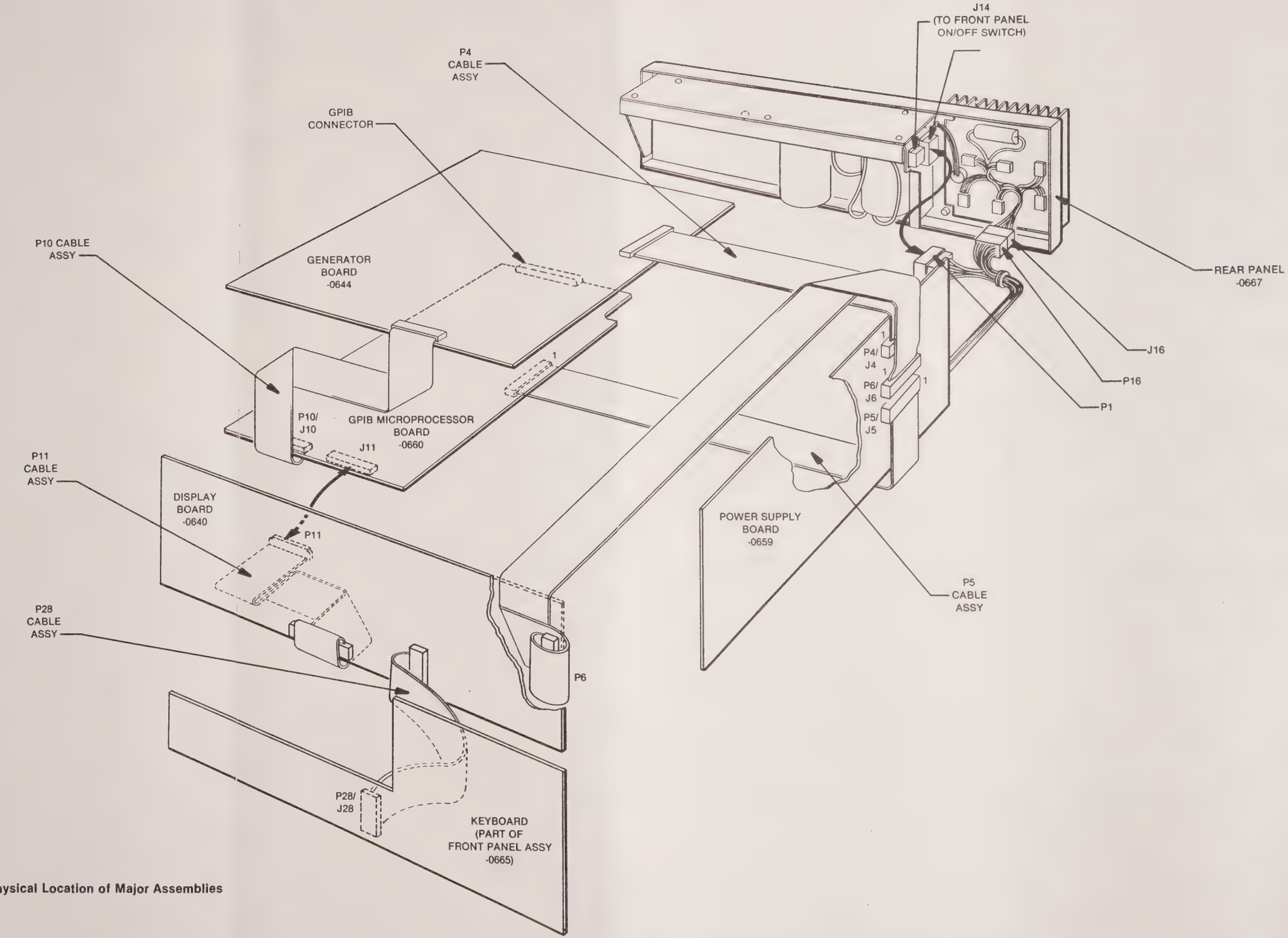


Figure 5-1. Physical Location of Major Assemblies

SECTION 5
CIRCUIT DESCRIPTION

5.1 BOARD FUNCTIONS AND CONNECTIONS

The circuit board assemblies and their connections are shown in figure 5-1. The functional elements and their relationship are shown in figure 5-2. The generator is the source of the output analog waveforms and the digital-to-analog circuits that evolve them. The microprocessor is the central processor which receives information from the GPIB, keyboard and generator and acts on these inputs as directed by its PROM stored data to issue commands and data for the desired output signals. The keyboard, display and the General Purpose Interface Bus (GPIB) are the links to the controller of the Arb. The GPIB interface interfaces the microprocessor with the remote controlling unit located on the GPIB: a minicomputer, calculator, etc. The interface detects when the Arb is addressed and makes the proper connections to receive data and transmit data. Optical couplers maintain circuit isolation between the GPIB and the Arb.

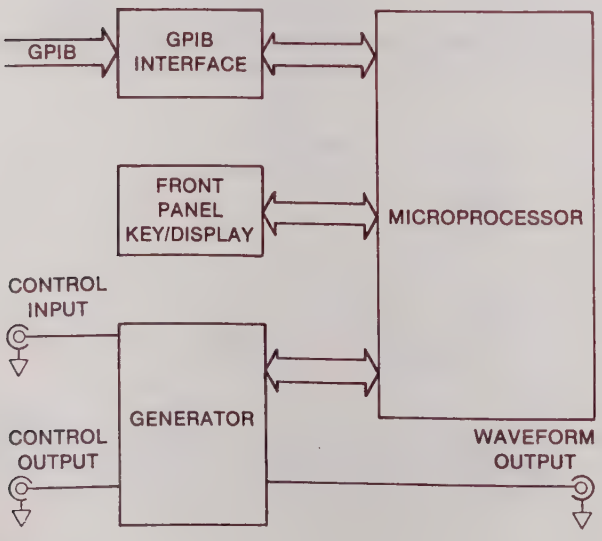


Figure 5-2. Basic Arb Block Diagram

5.2 GENERATOR

5.2.1 General

The Arb's generator is a source of various arbitrary waveforms which are produced by digital data processing and conversion to analog signals by digital-to-analog (D/A) converters. Its relationship to the other Arb basic blocks is shown in figure 5-2.

5.2.1.1 Basic Waveform Generation

The basic waveform generator is shown in figure 5-3.

If the clock frequency is fixed at 256 kHz and the counter divides by 256 (counter output is 8 binary bits incremented to count 256 steps), then the resultant waveform after D/A conversion circuit is a linearly increasing ramp at 1 kHz repetition rate.

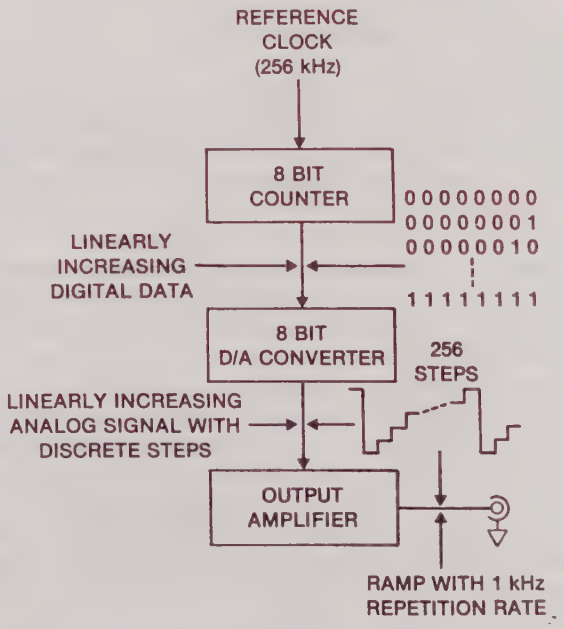


Figure 5-3. Basic Waveform Generator

When a digital data modifying circuit (solid state memory) is inserted between the counter and the D/A converter (see figure 5-4), the linearly increasing digital data are used to address the corresponding data locations in the memory.

Since the memory location is successively incremented by one count and the output is the contents of the memory location, the data applied to the D/A converter is independent of the counter output. Then, the counter output becomes simply a pointer to a specific location in the memory circuit. This is the basic operation of the arbitrary waveform generator (see figure 5-4).

5.2.1.2 Frequency Control

Figure 5-5 shows a fixed clock frequency of 256 kHz. When the clock frequency is divided by an 8 bit counter, 256 discrete sample steps are generated. Thus, the output frequency is 1/256 of the reference frequency, or 1 kHz.

If the reference frequency is not fixed at 256 kHz and can be selected, the output waveform frequency will follow at 1/256 of the reference. For example, if an output waveform at 2 kHz is desired, a reference clock of 512 kHz is required.

5.2.1.3 Waveform Smoothing

For low frequency operation of the Arb, it may be desirable to minimize transition steps between successive steps. This is the smoothing function. The basic operation of the smoothing circuit is shown in figure 5-6.

Drawing 1 shows the basic waveform steps created by 256 sample times. If the subtraction of digital data ($\triangle = |A - B|$) is accomplished in time to correct the step change and, if a linearly changing ramp is created as shown in drawing 2, it is possible to sum the opposite-sign and equal-magnitude signal (drawing 2) with the original signal (drawing 1) to cancel the step A to B while creating the smooth transition of A to C. The method to create the amplitude varying ramp is similar to figure 5-3, except the reference voltage for the D/A converter changes as the step size is computed.

The 100 small steps of ramp must be generated by a 100 times higher clock frequency than the basic waveform steps. Therefore, the smoothing method is an inherently low frequency operation.

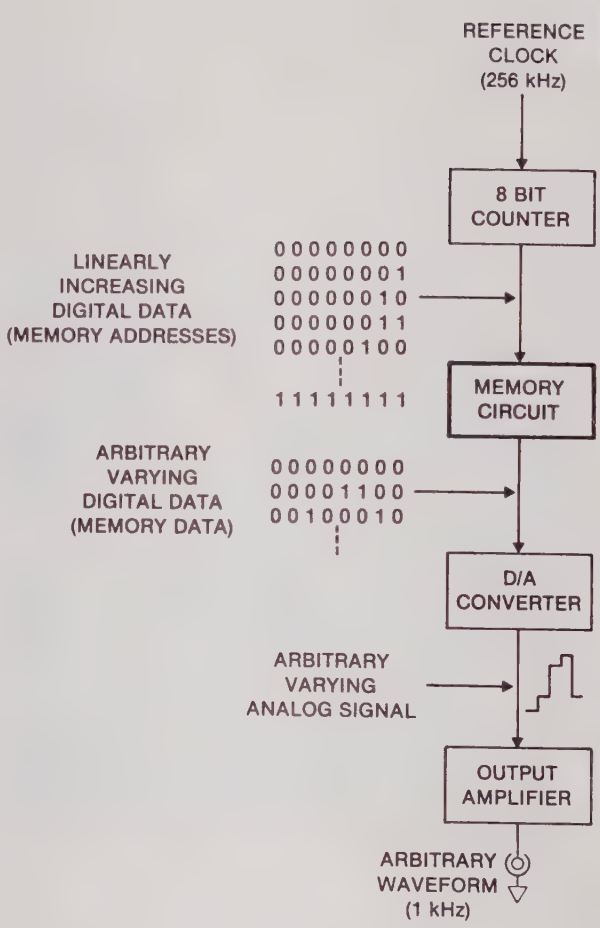


Figure 5-4.
Basic Waveform Generator With Memory Circuit

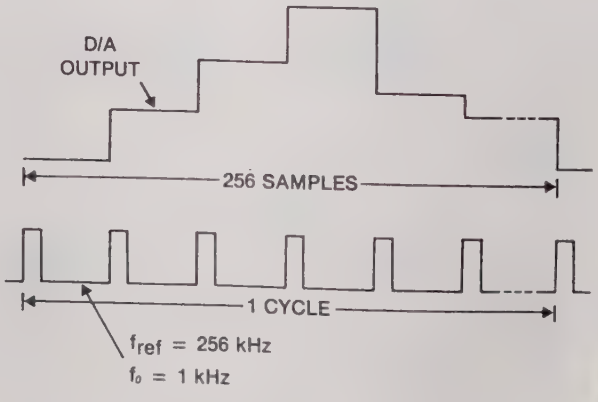


Figure 5-5. Clock/Waveform Frequencies

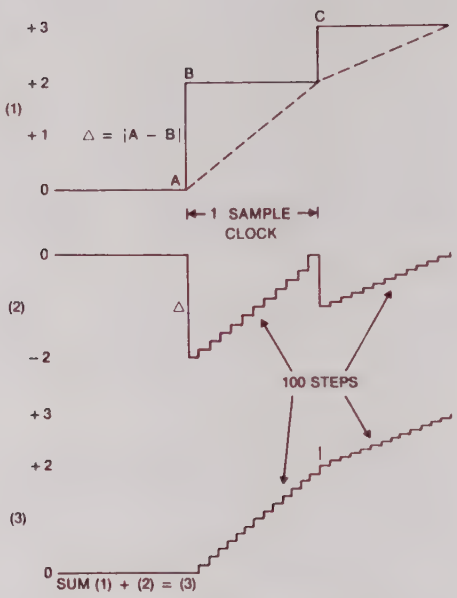


Figure 5-6. Smoothing

5.2.1.4 Summary

The arbitrary waveform is created on a 256 X 255 coordinate grid, amplified, dc offset and attenuated (figure 5-7).

5.2.2 Generator Circuits

The theory of specific generator circuits is given in this paragraph. The relationship of each circuit to the other generator circuits is shown in figure 5-8.

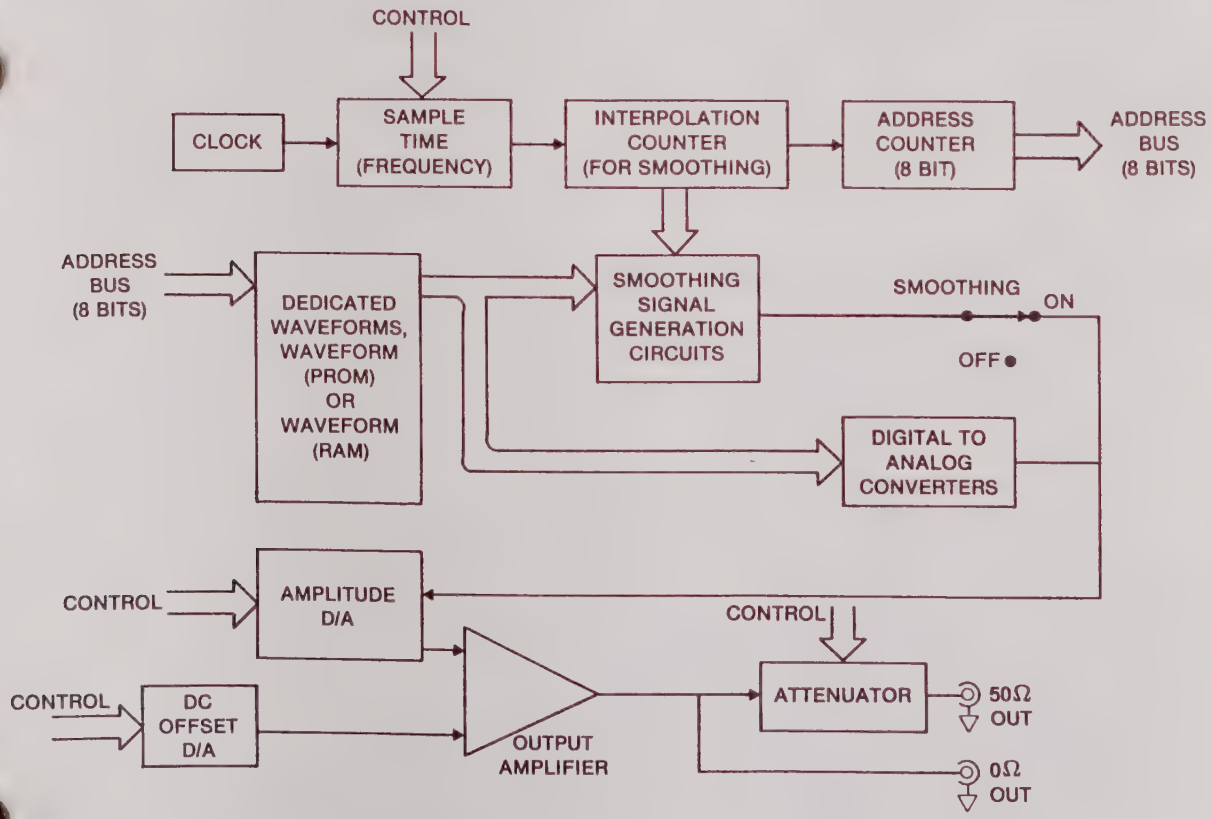


Figure 5-7. Simplified Generator Block Diagram

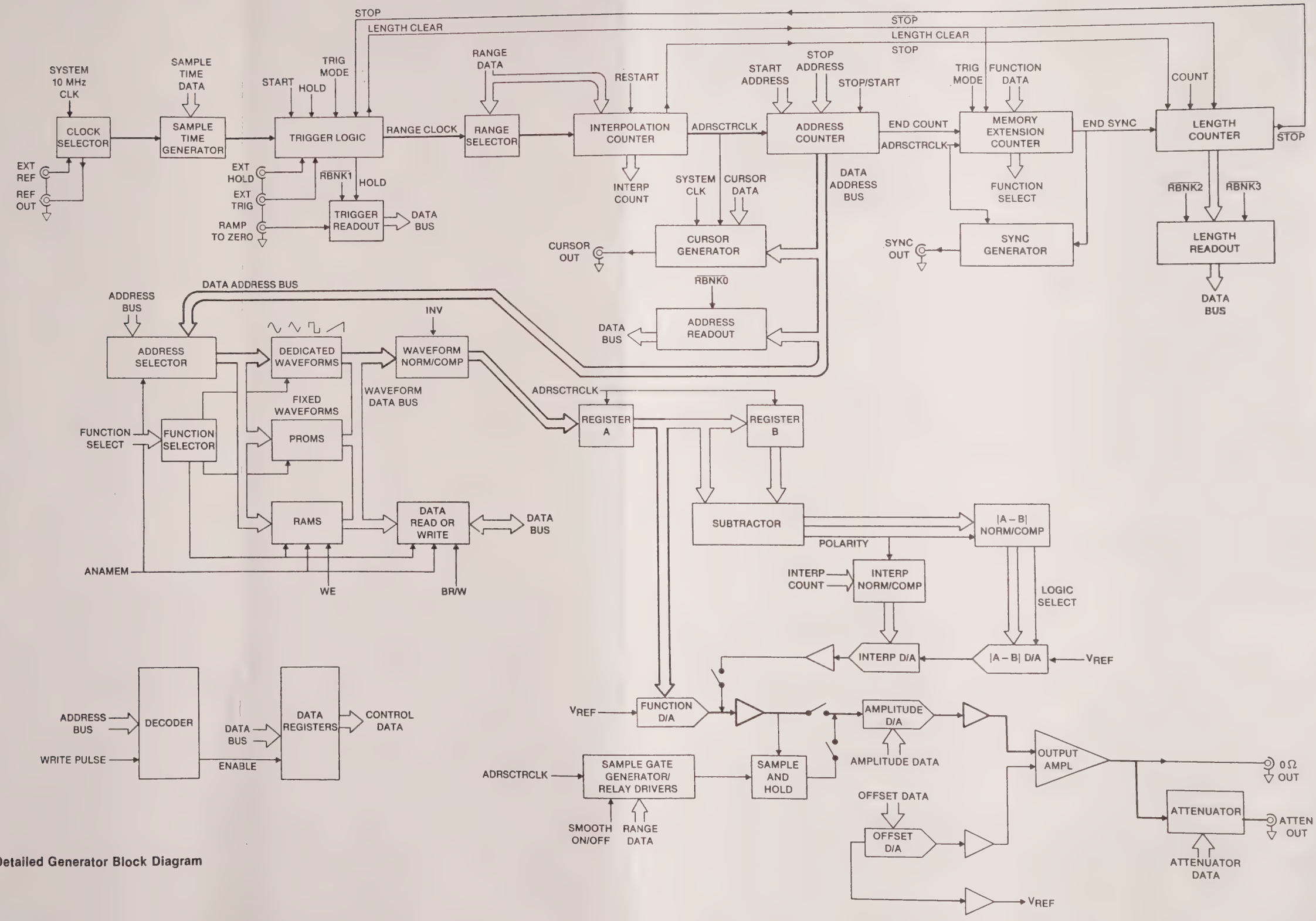


Figure 5-8. Detailed Generator Block Diagram

5.2.2.1 Sample Time Generator

The sample time generator is a conventional programmable counter. When the input reference frequency is fixed at 10 MHz, the time interval is 100 nanoseconds (see figure 5-9). If the counter divides the reference frequency by N (multiplies reference period by N), the output frequency f_S is f_r/N and the output period t_S is $t_r \bullet N$ or $100 \bullet N$ nanoseconds. So, if N is set to 3, then the output period of the sample time generator is 300 nanoseconds; thus, data sample time base is generated in 100 nanosecond increments.

The Arb is programmed in terms of the number of digital samples for a waveform and elapsed time per sample. When 100 samples constitute a waveform and each sample time is programmed to 1 μs, then 100 μs will complete the waveform data block sampling. Then, the block rate or waveform frequency is 1/100 μs = 10 kHz. If, as shown in figure 5-10, the number of samples is reduced to 50, while maintaining the same sample time, then the waveform frequency will increase to 1/50 μs = 20 kHz.

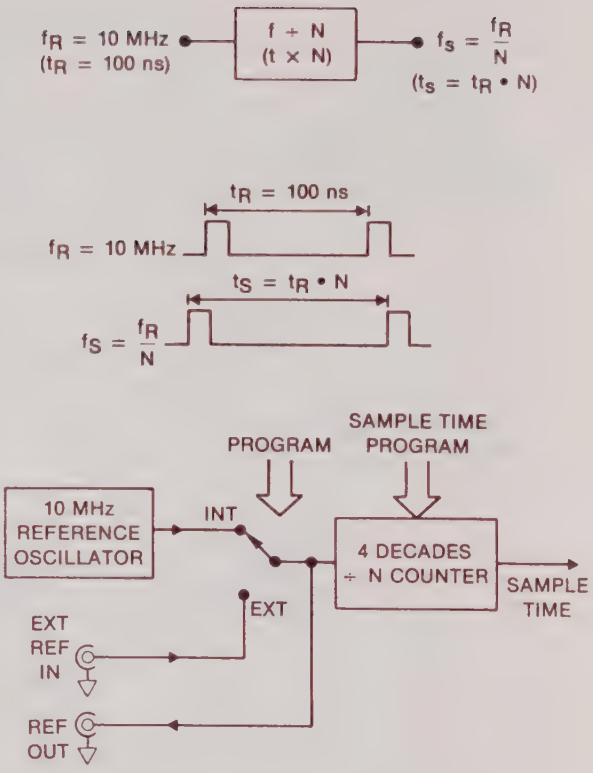


Figure 5-9. Sample Time (t_S) as Increments of Reference Time (t_R)

5.2.2.2 Trigger Logic

The trigger circuit controls the number of waveform cycles to be output. This circuit works in two modes. The first mode is a preset (burst) mode. By simply counting the overflow bit of the address counter (see figure 5-11) and programming the counting length, the trigger circuit will start and stop at the predetermined address after the preset number of cycles are output.

For the monitor mode, the sample time gate will pass all the timing pulses after the trigger signal is applied until the hold pulse forces the gate to stop outputting sample time pulses to the address counter. This is an asynchronous, instantaneous operation and the output waveform stops immediately. The number of output cycles is monitored by the same length counter used to control the preset waveform cycles.

5.2.2.3 Address Counter

A unique feature of the Arb is the precise control of the start/stop addresses. Normally, the address starts at 0 and stops at 255, thus repeating the entire 256 addresses. However, the start/stop counter is programmable for a set of arbitrary start and stop addresses when required.

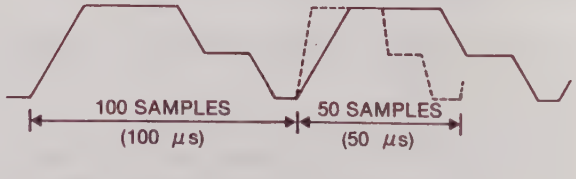


Figure 5-10. Constant Sample Time and Reduced Number of Samples

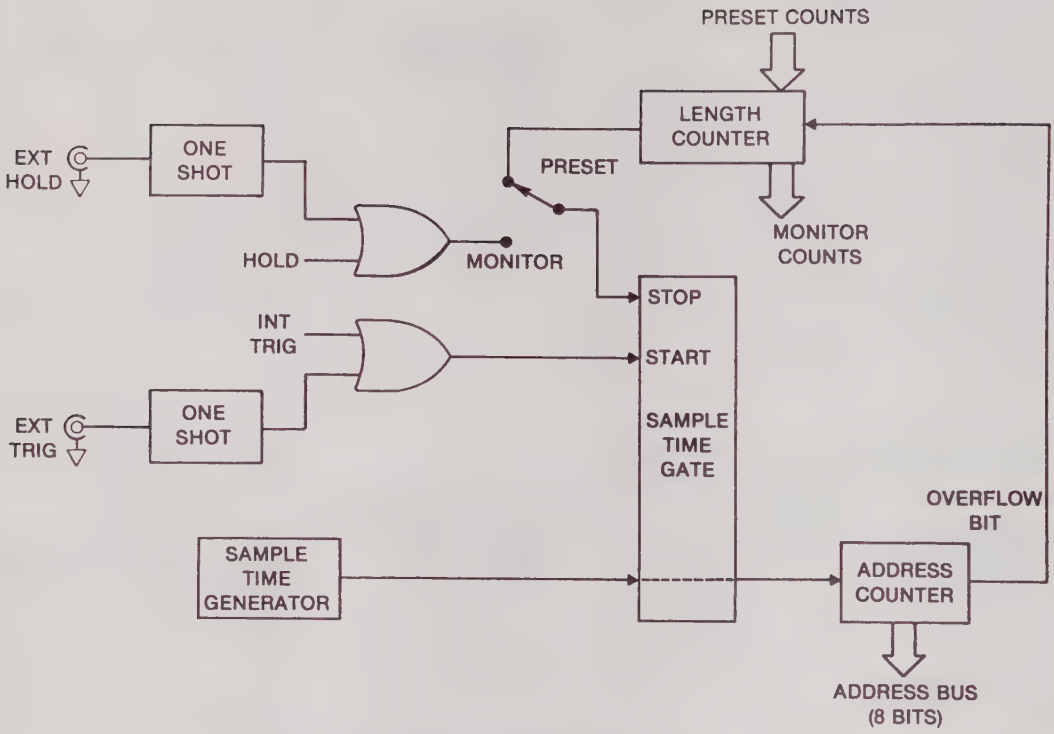


Figure 5-11. Trigger Circuit

Figure 5-12 shows the simplified start/stop address scheme for the partial block mode. The load input of the programmable address counter is used to set the start address. When the counter counts up to the preset stop address, the comparison of the programmed preset address with the counter output is made by a comparator (array of "exclusive-OR" gates). If the two addresses match, the output becomes true state. Thus, when all eight bits of the counter output are compared to the programmed stop address and match the data, the start address is loaded to the counter when load command is given. Therefore, the address counter starts and stops at any programmed addresses.

5.2.2.4 Memory Extension Counter and Function Selector

The memory extension counter is a programmable sequencer to be used for stacked PROMs or RAMs. Whenever the address counter reaches the end point (either STOP ADRS or 255), an end count pulse is generated. If function selection is programmed to memory extension (stacked PROMs or RAMs), the pulse is monitored and counted by the programmable memory extension counter (see figure 5-13).

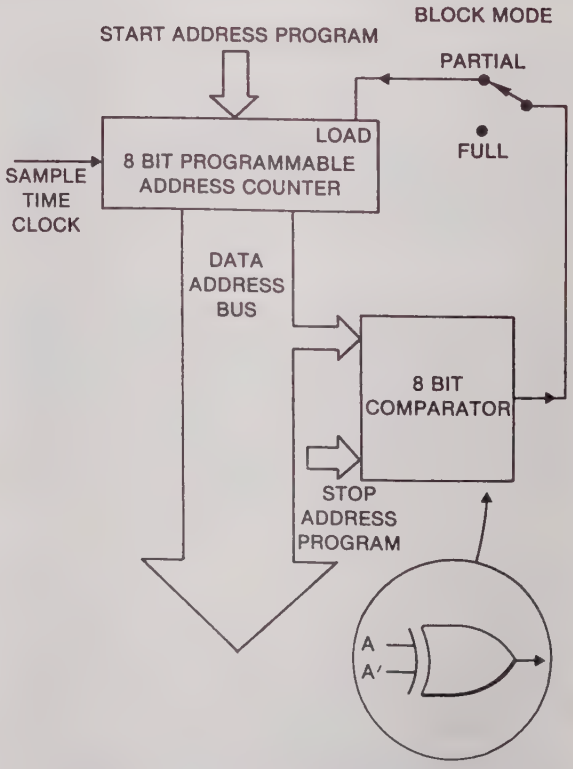


Figure 5-12. Waveform Start/Stop Control

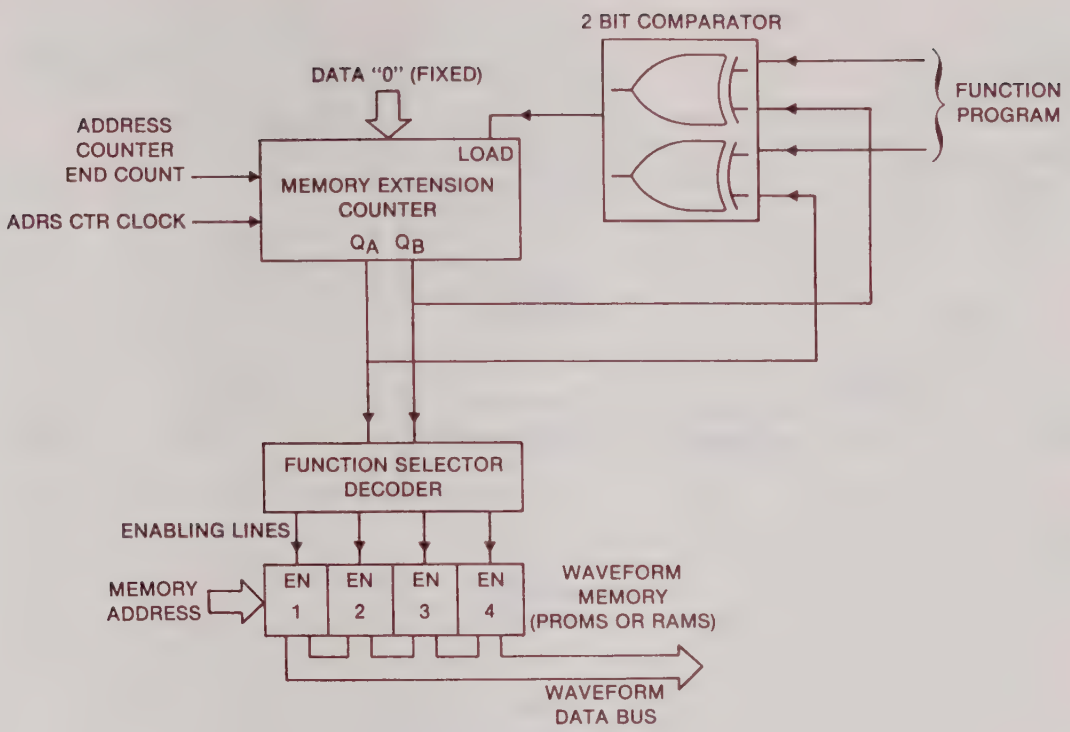


Figure 5-13. Memory Extension

When the counter output matches the function program, data "zero" is synchronously loaded to the counter. This will force the counter to reset to zero. Thus, the output of the counter repeats between zero and the function program (up to three). The output is decoded and used to sequentially multiplex and enable the PROMs or RAMs in block increments.

5.2.2.5 Length Counter

The length counter functions as detector of the preset burst count or the count monitor, when the instrument is set to trigger mode. It is a four decade decimal counter with an output comparator and data bus drivers (see figure 5-14). When the mode is set to preset length, the counter accumulates the sync pulse (or the pulse at the last address) until the output matches preset numbers at the input of the comparator. Then, the comparator output will set the sample time gate flip-flop to the off state, thus forcing the address counter to stop at the last address.

When the instrument is set to the monitor mode, the counter accumulates the whole number of waveform cycles, from 1 to 9999.

In both modes, the output state of the counter is read by the microprocessor through the data bus.

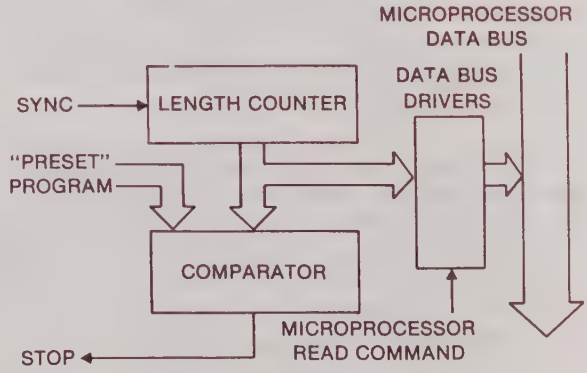


Figure 5-14. Length Counter

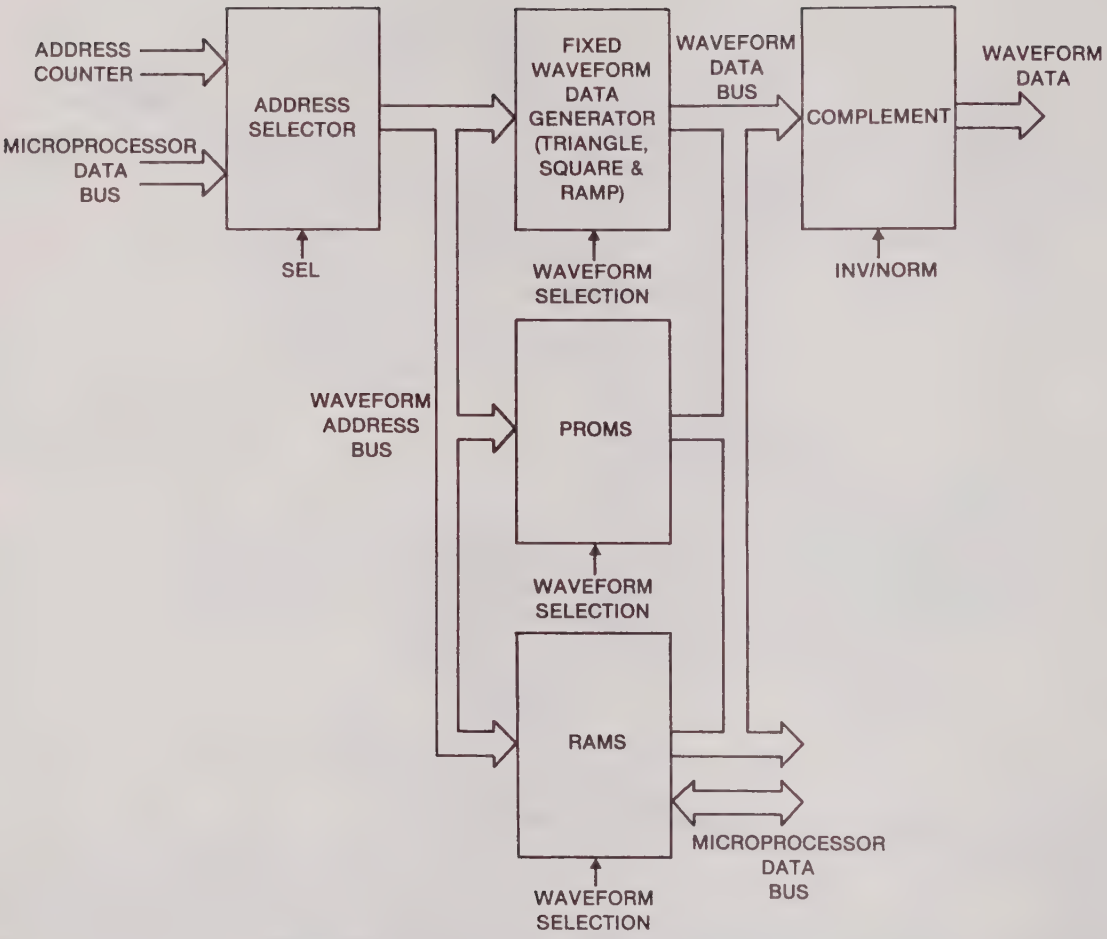


Figure 5-15. Waveform Data Generation

5.2.2.6 Waveform Data Generation

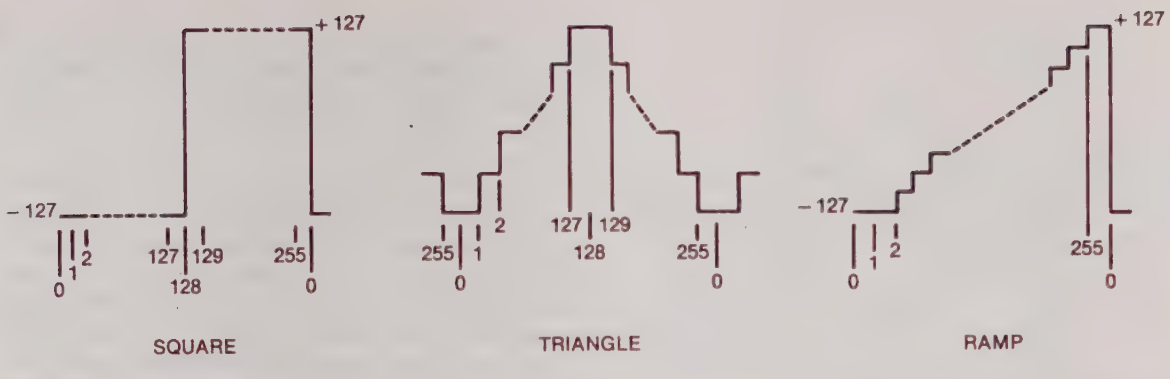
All the waveform data are stored either in programmable read only memories (PROMs) or in random access memories (RAMs) with the exception of triangle, square and ramp (see figure 5-15).

The triangle, square and ramp waveform data are generated by logic manipulation of the address data. For the square wave, the most significant bit of the 8 bit counter is used. It is zero for counts 0 through 127, then one for counts 128 through 255. These two states are translated to block amplitudes of -127 and $+127$, respectively.

For the triangle waveform, the most significant bit is not used; only seven bits are used. The 0 through 127 counts take 127 of the 255 amplitude steps, 2 at a time, to form the first leg of the triangle. The 128 through 255 counts are complemented by a circuit and form the mirror image of the first 0 through 127 counts to form the second leg of the triangle waveform. Notice that the triangle stays at 127 for 2 counts and -127 for 2 counts.

For the ramp waveform, the incrementing 8 bit output from the counter steps out a ramp as shown in figure 5-16. Because there is one more count (256) than block amplitude levels (255), a special circuit causes both count zero and count one to map a -127 block amplitude, as shown in the figure.

A fourth fixed set of waveform data generates a sinusoidal waveform. This is a special case of PROM programmed arbitrary waveform data. The waveform address points to the memory location, while the corresponding data are output to the waveform data bus.



Address$_{10}$	Address$_2$ MSB	Bit Conversion (Ramp Only)	Mapping Square	Mapping Ramp	Mapping Triangle
0	0 000 0000	0000 0001	– 127	– 127	– 127
1	000 0001			– 127	– 125
2	000 0010			– 126	– 123
		Complement (Triangle Only)			
127	0 111 1111		– 127	– 1	127
128	1 000 0000	111 1111	127	0	127
129	000 0001	111 1110		1	125
130	000 0010	111 1101		2	123
255	1 111 1111	000 0000	127	127	– 127

Figure 5-16. Counter Generated Waveforms

In this case, sinusoidal waveform data are sequentially stored in the memory location 0 through 255. In a similar manner, if a set of customer defined waveform data is stored in a PROM, the output data are that customer's data sequence.

The random access memory (RAM) is a data storage device which can store (write in) or output (read out) data at any address. The function is very similar to PROMs when data are output; in addition, the RAM data content may be changed at any address.

All the waveform data on the bus can be complemented.Inverted waveform data can be selected by programming a negative amplitude.

5.2.2.7 Interpolation Counter

The sample time generator increments the address counter by one whenever a sample time pulse is output. By inserting a divide by 100 counter in the path, the address counter clock can be divided by 100 while generating 100 interpolation clock pulses for each sample time pulse (see figure 5-17). The interpolation steps are used to create the 100 interpolation steps during each sample time for waveform smoothing.

5.2.2.8 Smoothing and Waveform Generation

The digital waveform data bits are synchronized to the address counter clock and stored by registers A and B.

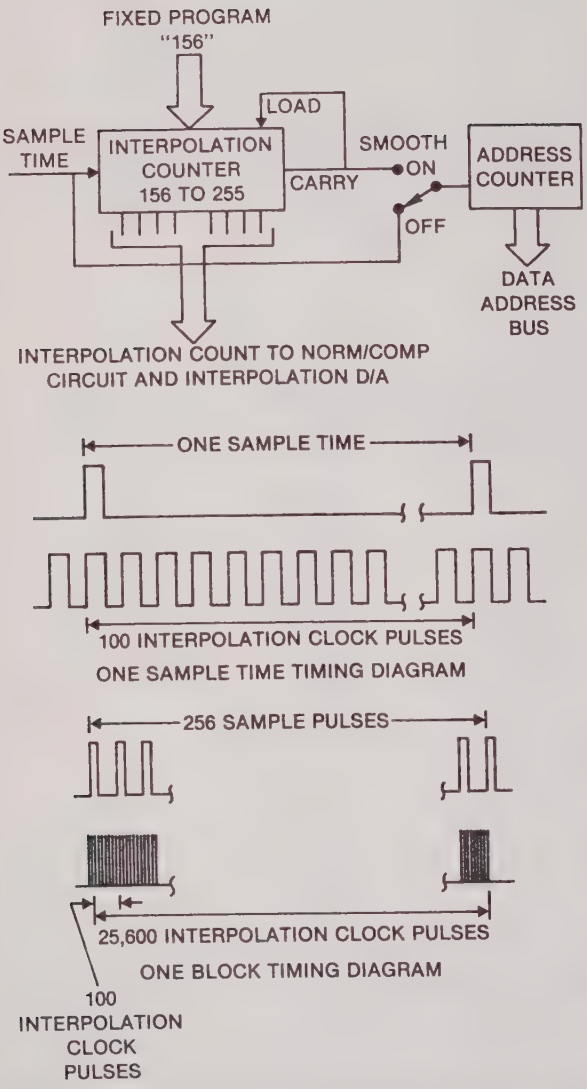


Figure 5-17. Interpolation Counter

The register A output is applied to a function D/A input to generate bipolar current proportional to the digital data (see figure 5-18). The other two paths feed to the inputs of the B register and |A − B| subtractor. These data are involved in waveform smoothing and are used only if smoothing is programmed. The B register output is the complement of register A and delayed by one sample time. These data in registers A and B enable the subtractor circuit to compute amplitude differences of the adjacent sample time steps. Feeding the |A − B| subtractor digital data into the |A − B| D/A generates unipolar proportional current which feeds to the reference input of the interpolation D/A. The interpolation counter output (refer to paragraph 5.2.2.7) is connected to a circuit which prepares it for interpolation D/A use.

The interpolation D/A is driven by the interpolation counter to create a 100 step ramp. The desired ramp will either be from a positive level to zero or from a negative level to zero. The starting level of either ramp is determined by feeding the |A − B| D/A output amplitude to the interpolation D/A reference. By the nature of the D/A device used, a binary count from 28_{10} to 127_{10} is required for a 100 step negative level to zero ramp, and 227_{10} to 128_{10} for a 100 step positive level to zero ramp (see (a) of figure 5-19).

Since the output of the interpolation counter is 156_{10} to 255_{10} (b), which is not in the correct form for the D/A input, it must be adjusted to be in the proper range. The most significant bit is removed by using only the least significant 7 bits (c). At the complement circuit, a binary zero is added for the MSB when a negative level to zero ramp is required (d). When a positive level to zero ramp is required, the 7 bits of the interpolation counter are complemented (e) and a binary one is added for the MSB (f).

The amplitude (or slope) of the ramp is controlled by the reference current fed by the |A − B| D/A, while the direction of the slope is controlled by the polarity signal fed to the complement circuit.

If smoothing is not selected, the function D/A output current is converted to a proportional voltage change by the summing amplifier. When smoothing is selected, in addition to the function D/A output, the 100 step correction ramp is fed to the summing node of the summing amplifier, thus creating a smooth analog transition for the discrete step (see figure 5-20).

The resultant output waveform contains large transients due to two opposing and equal magnitude signals cancelling each other. In order to minimize these transients, a sample and hold circuit is inserted in the path between the output of the summing amplifier and the amplitude control D/A whenever smoothing is selected. The sample and hold circuit follows the input signal all the time, except the transient interval of 400 to 500 ns. Since the transient occurs synchronous to the rising edge of the address counter clock, the sample and hold circuit disconnects the input signal and holds the prior level long enough to avoid the transient condition (see figure 5-21).

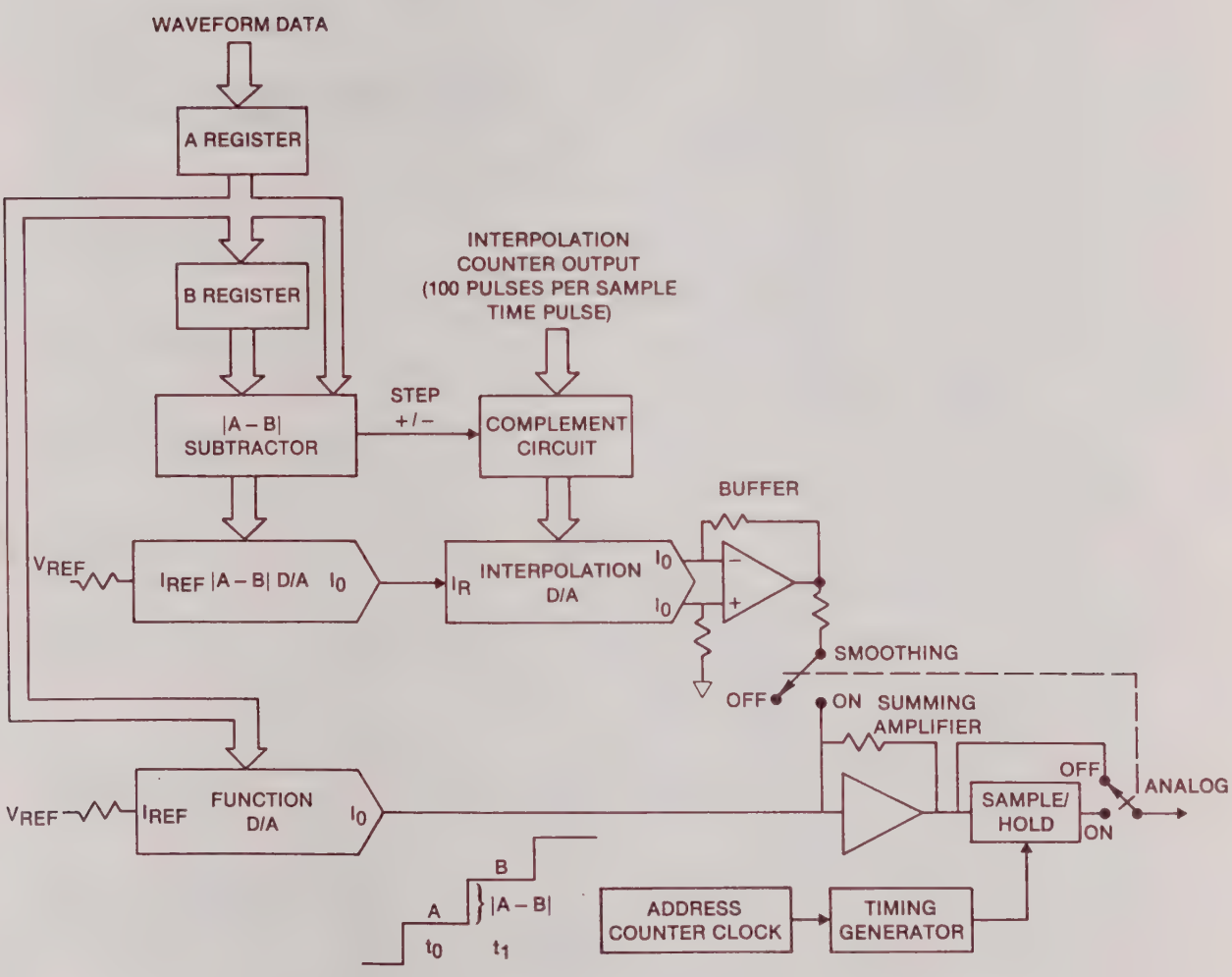


Figure 5-18. Smoothing and Waveform Generation Block Diagram

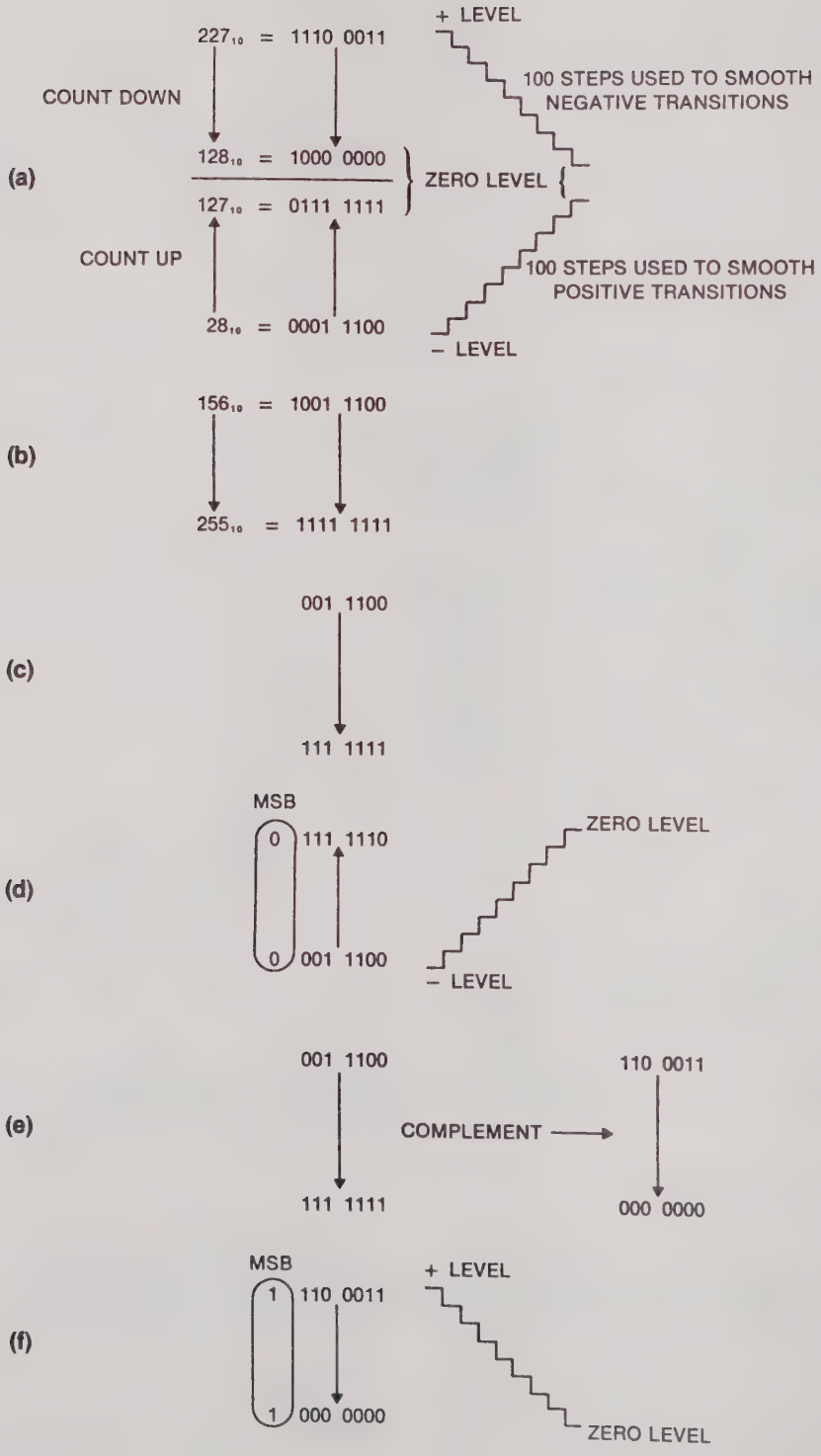


Figure 5-19. Interpolation Data Preparation

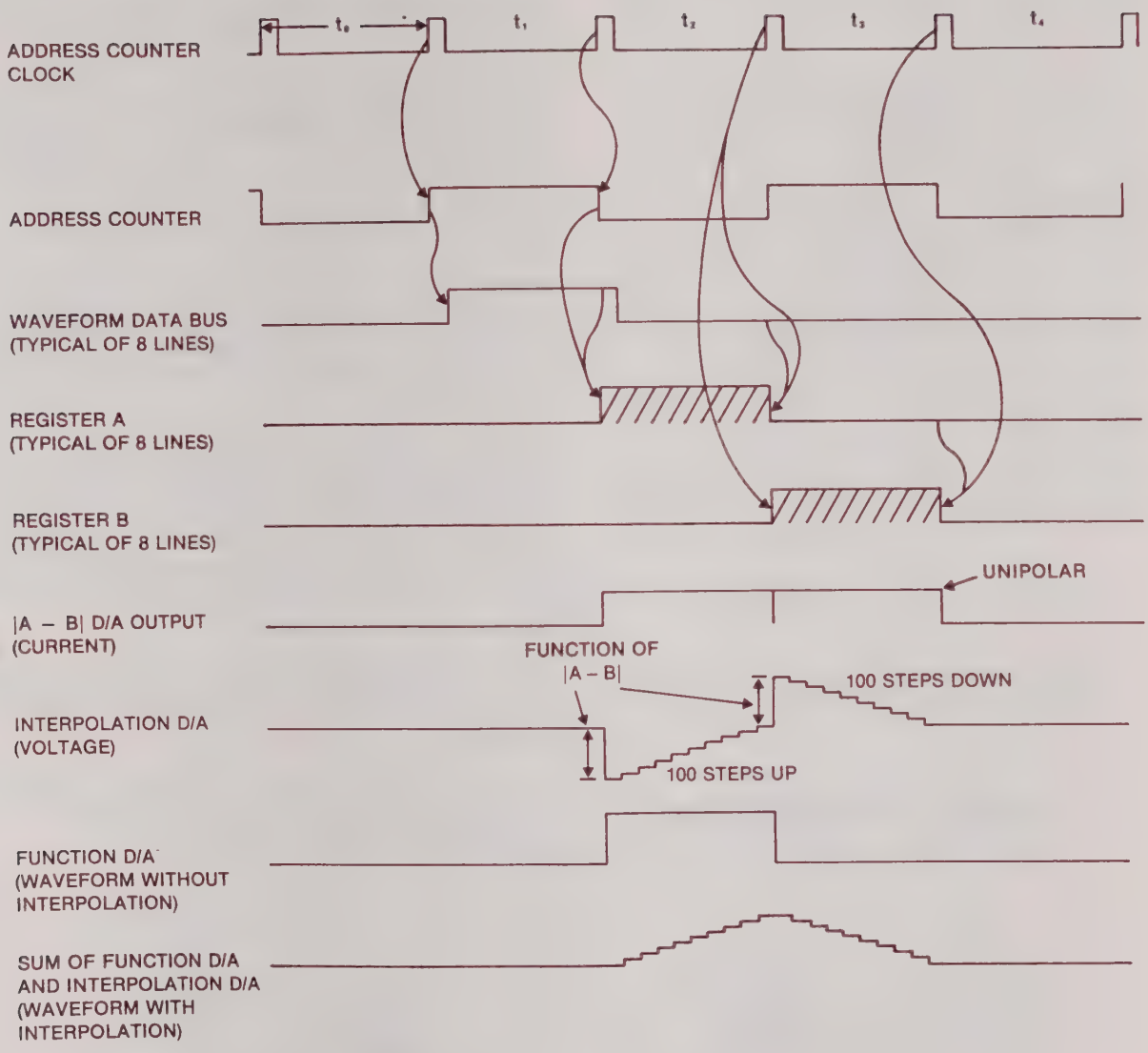


Figure 5-20. Waveform Generation Timing Diagram

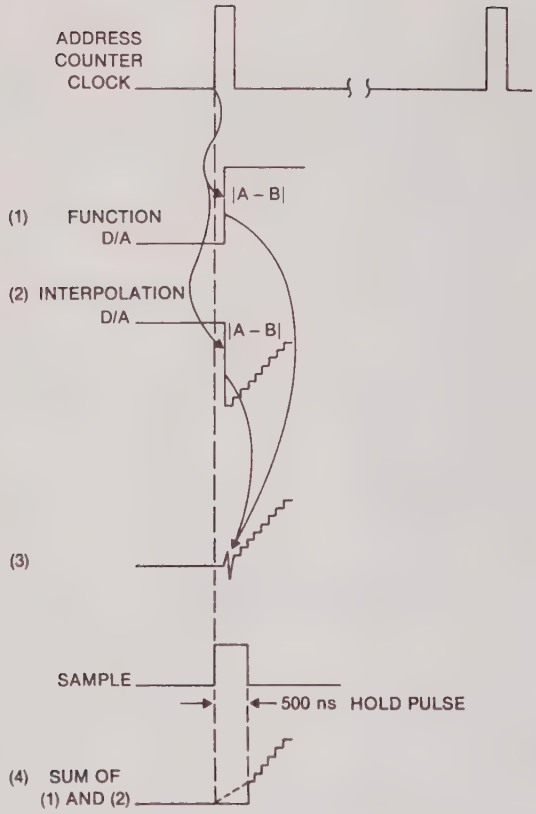


Figure 5-21. Transient Elimination

5.2.2.9 Output Stage

The output amplifier consists of an amplitude D/A, dc offset D/A, power amplifier and output attenuator (see figure 5-22).

The amplitude D/A is an integrated resistor ladder network with CMOS switches. The input analog signal is attenuated proportionately by amplitude data. It works analogous to a variable resistance element controlled by the wiper position.

The dc offset D/A generates bipolar current proportional to the offset data. The current is added to or subtracted from the summing node of the power amplifier, thus causing the amplifier output to dc shift proportionately.

The power amplifier is an inverting dc amplifier with feed forward connection. For dc stability, the connection is made to the emitter of Q5 through a zener diode from emitter follower Q4. (Refer to schematic -0644.) The high frequency signal bypasses the dc path and connects the output bias transistors through the two feed forward capacitors.

The output attenuator consists of simple voltage dividers with 50 Ω output impedance selected by reed relays.

The low impedance output (0 Ω OUT) is provided directly from the output of the power amplifier.

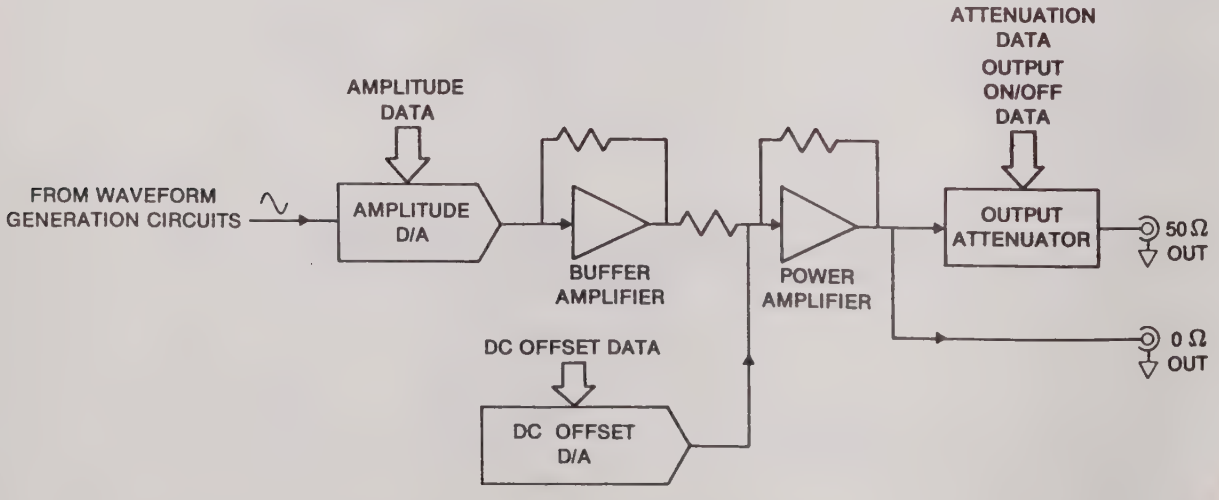


Figure 5-22. Output Stage

5.3 DISPLAY AND KEYBOARD

5.3.1 Display

The display consists of the status indicating individual LEDs, the "label" and "units" characters in two 5 × 7 LED dot matrices, and the seven numerals made up of the 7-segment LEDs.

The label and units dot matrix LED drivers are divided into row and column drivers (see figure 5-23). Data for each dot matrix is stored in the display data registers. The divide by 10 BCD counter output is decoded into 10 decimal lines grouped in even and odd numbers. Even numbered ones drive label columns, while odd numbered ones drive units columns. This allows even distribution of the on-time of each column for each dot matrix, thus evenly illuminating the display. The column driver sequentially points to one column, then another, alternating between the label and unit matrix. The row driver will then designate which LEDs will light in each particular column. The least significant bit of the BCD counter multiplexes the two data register outputs synchronous to the odd/even column switching.

The PROM stores row data for characters required by the dot matrices and five input lines to the PROM from the data registers are dedicated to designating the characters (32 maximum). The multiplexer feeding those five lines is alternately switched between the designated label character and the designated unit character. Now that the unit and label characters are designated, the three lower bits of the 8 bit PROM input signify the column. These three bits are the three upper bits of the BCD counter. They count 0 to 4, with two count periods for each count. The PROM is thus addressed for label column 1 and transmits seven bits of row data; then units column 1 and transmits seven bits of row data; then label column 2, etc. By addressing the upper five bits of the PROM and sequentially addressing the lower three bits, the label and unit characters are displayed.

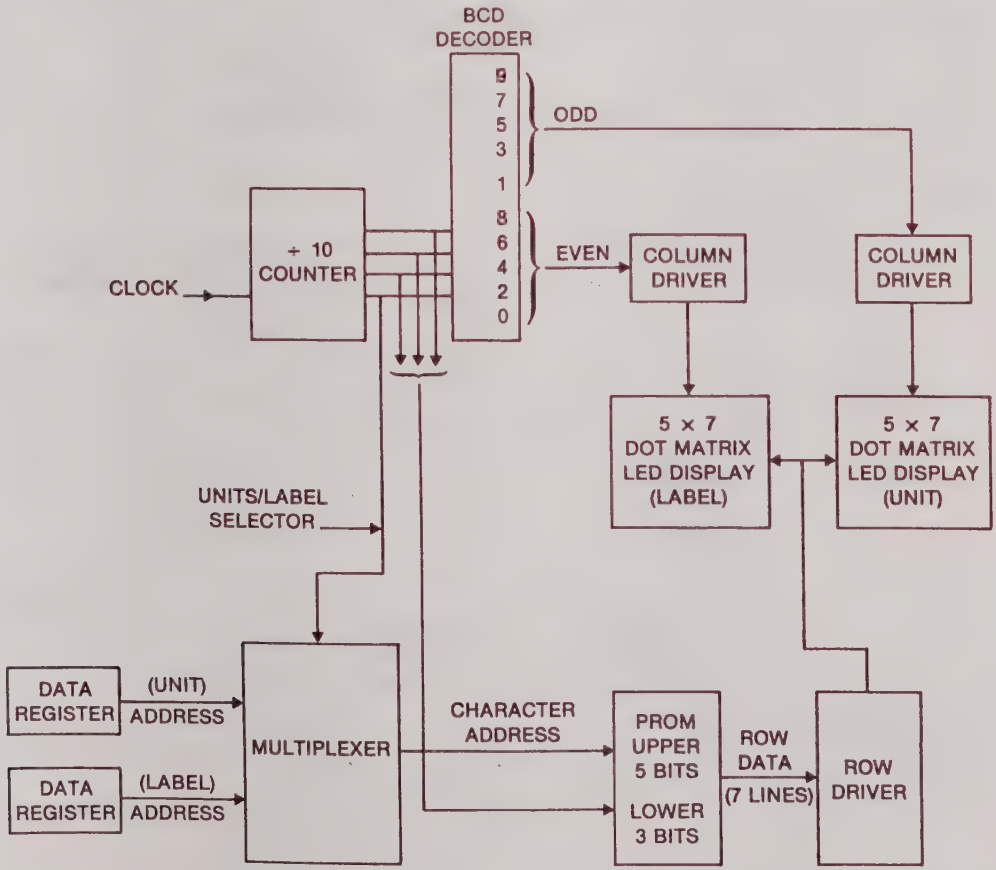


Figure 5-23. Label and Units Display Diagram

The numerical display consists of seven 7-segment LED displays. The numerical information to be displayed is stored in a Random Access Memory (RAM) located on the display board (see figure 5-24). When WBNK 7 (write bank 7) is selected and the lower four bits of data and the address are present, the information is entered into the RAM by applying the write enable pulse (WE). Once the data are stored at the respective addresses of the RAM, the contents can be sequentially output to the PROM input. A 2 kHz oscillator clocks a divide-by-eight counter which furnishes sequential 3 bit read addresses to the address selector. When write enable is false, the RAM operates in read mode using the sequential addresses. RAM output is a BCD code for one of 15 possible display characters plus blank. The PROM converts BCD to 7-segment data.

The 3 bit read addresses are also decoded to 8 bits, 7 of which sequentially furnish grounds to the seven display digits. Each digit common is driven by the corresponding buffered output of the BCD-to-decimal decoder.

The status displays consist of individual LED lamps. The data are stored in the registers after the lower 3 bits of address bus and the selected write bank (WBNK5) generate corresponding clocks for the registers.

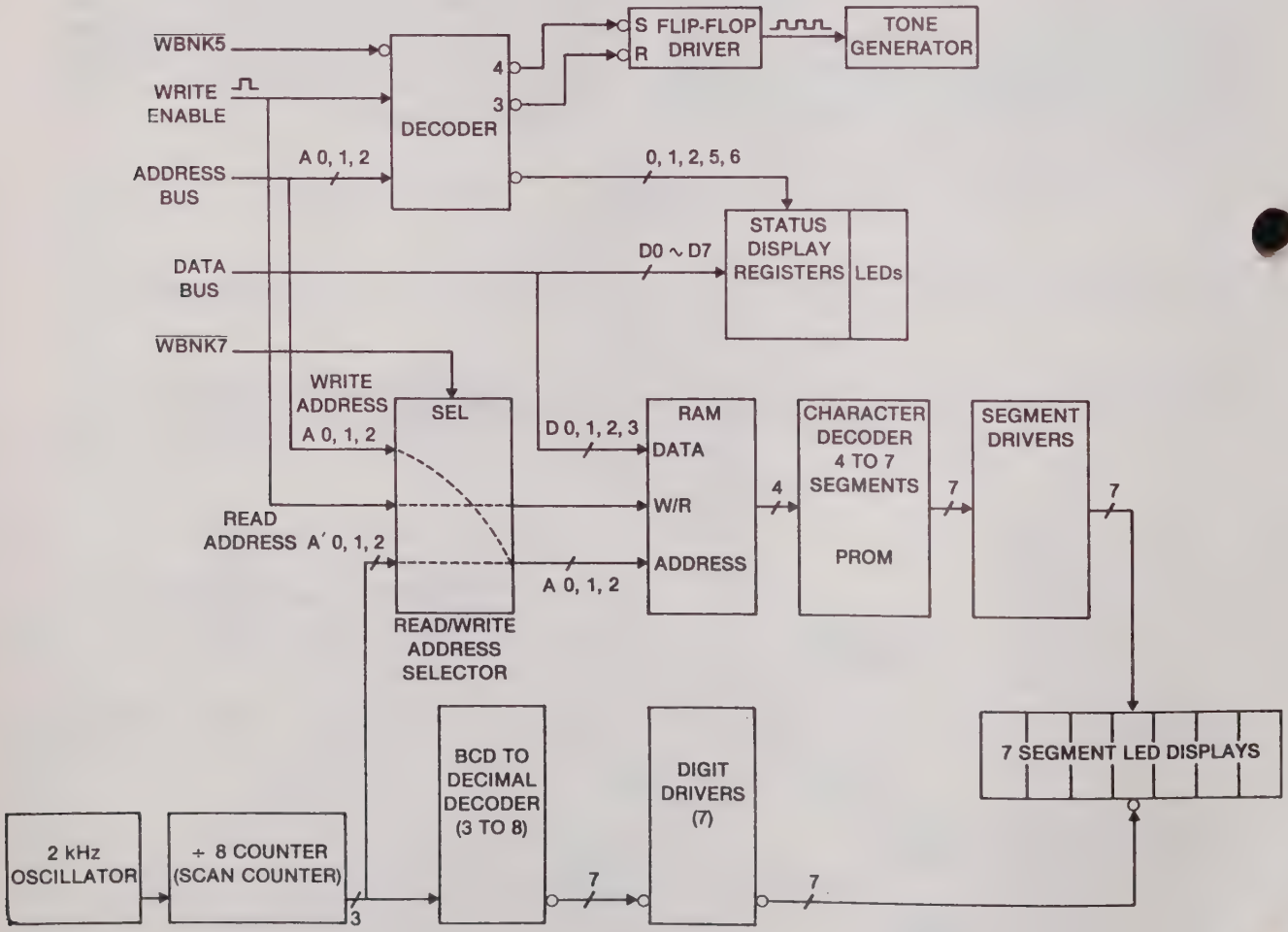


Figure 5-24. Numerical Display Diagram

5.3.2 Keyboard

The keyboard consists of the printed circuit switches arranged in a 6 × 8 crosspoint array (see figure 5-25). Periodically, the microprocessor, under program control, sends a read pulse ($\overline{\text{RBNK4}}$) to the keyboard logic. The pulse advances the divide-by-eight counter whenever a pulse transition of high to low state occurs. The counter output state is indicated on the data bus (D3, D4, D5), since the bus driver is enabled by the low state of the read pulse. The counter output (one of eight states) is decoded and drives one of the six keyboard columns to low state (unless one of the two unused states are selected). If one of the keys is pressed, the priority encoder encodes the row number and indicates on the data bus (D0, D1, D2). The flag state is also indicated on the data bus (D7). When the microprocessor detects the new keyboard data, it scans again after 30 milliseconds. If the data remain the same, the key location data are entered and processed. The key depression indication may be fed back to the operator by the sounder on the front panel.

5.4 MICROPROCESSOR

The microprocessor acts as the control processing unit, receiving information from GPIB, the keyboard and the generator board; and acts upon these inputs as dictated by the software. Software directs the processor to address the Arb subsystems and issues commands and data which direct the generator to output the desired signals.

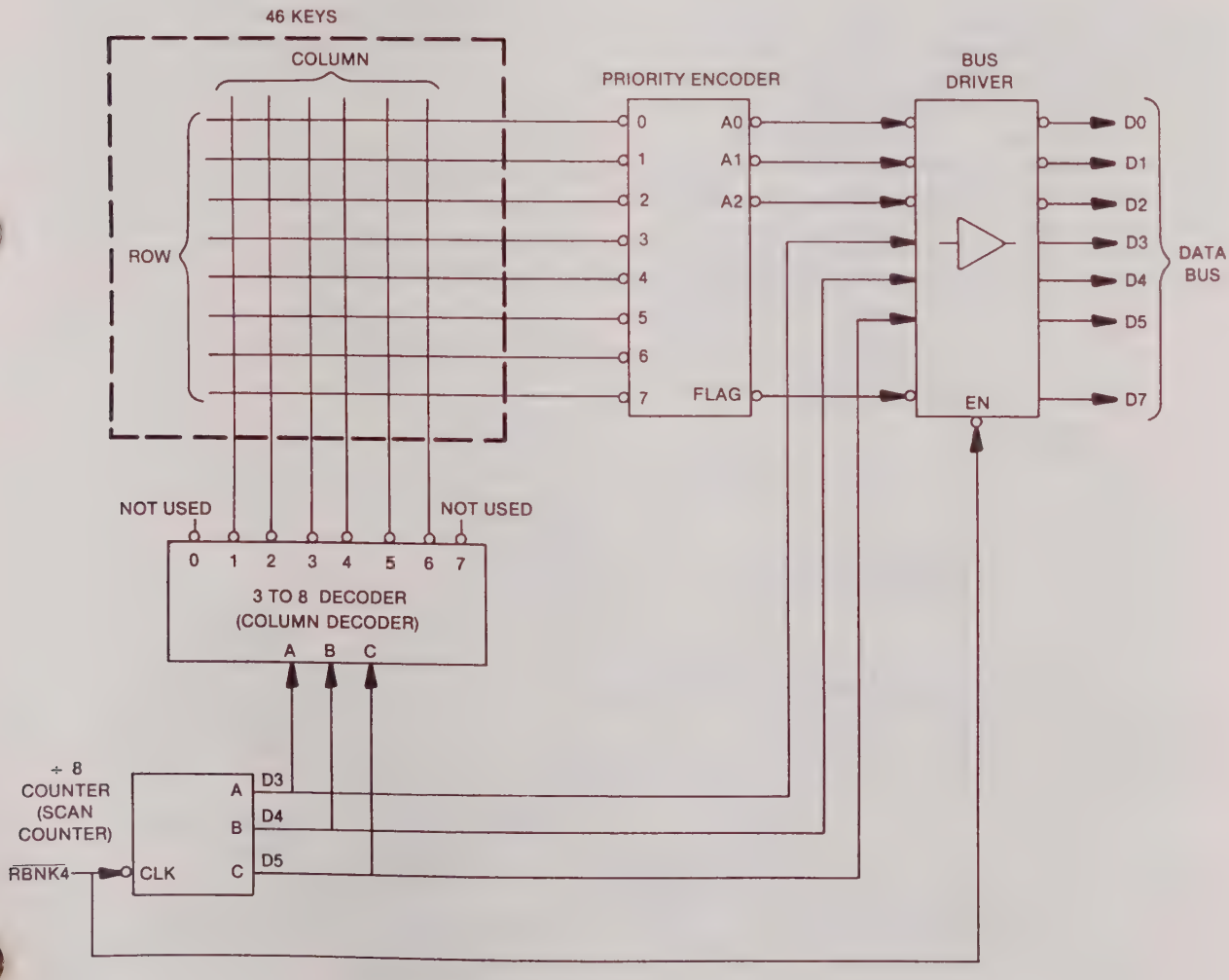


Figure 5-25. Keyboard Diagram

Software refers to a sequence of commands, called a program, which is executed by the microprocessor. This sequence of instructions, stored in PROM, commands the microprocessor to perform according to the Arb specification. All information transfer takes place under the control of the software. Programs are composed of machine language instructions, messages and tables which provide sequencing information. Program data from the PROM, temporary data from the RAM and input data from the keyboard, GPIB or generator board are connected to the microprocessor through interconnecting cables.

The microprocessor section of microprocessor/GPIB board contains an 8 bit processor, buffers, decoders, RAMs, PROMs and a 10 MHz, crystal controlled oscillator. Figure 5-26 shows the basic blocks of the microprocessor section. Address lines are buffered to the external subsystems, memories and decoders. Eight bit bidirectional data lines are received from and driven to the external subsystems. The memory data lines, which are 3-state outputs, connect directly to the microprocessor data bus. Control signals necessary to describe transactions are buffered and routed to subsystems. The 10 MHz clock pulses are generated and buffered to the generator board. The 1.25 MHz clock pulses are used as the microprocessor clock. 5 MHz and 1.25 MHz clocks are also used to run the GPIB interface.

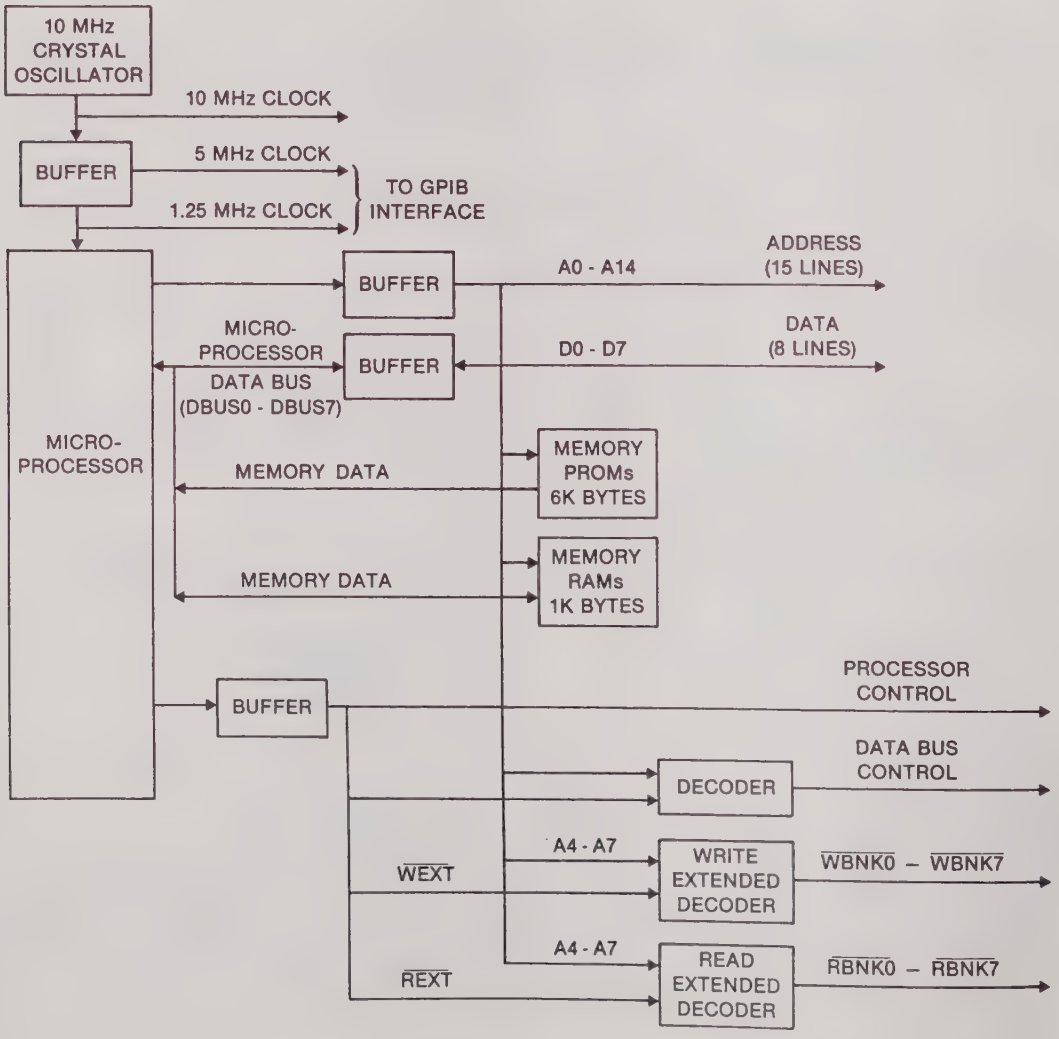


Figure 5-26. Microprocessor Block Diagram

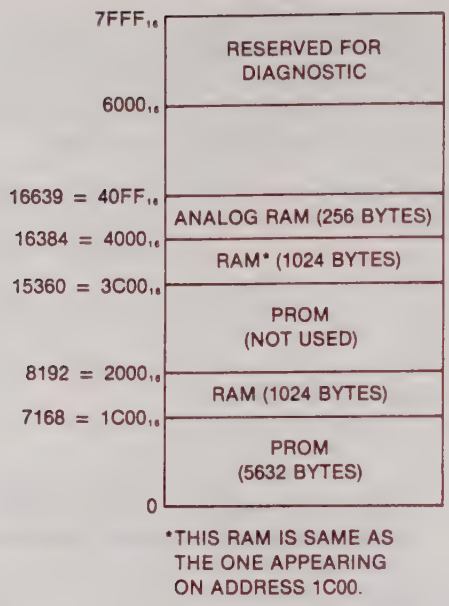


Figure 5-27. Memory Address Allocation

The PROM locations are accessed by the microprocessor by asserting an operation request with a read transaction. If the address is within the PROM space, data will be placed on the data bus.

A RAM read or write operation is initiated by the microprocessor issuing an operation request within the prescribed RAM address space. Since the RAM operates in static mode, data are accepted or presented immediately. The RAM stores the current setting, command strings, error reports and status.

The memory PROM contains 6144 bytes of fixed memory. Each of the three memory chips provides 2048 eight bit words. Addresses from the microprocessor are buffered and sent to each chip. The address allocation is shown in figure 5-27.

The read extended and write extended decoders (see figure 5-26) each generate eight read and eight write signals (RBNK0-7 and WBNK0-7) by decoding address lines A4 - A7. In Christmas tree fashion, each write bank signal (see figure 5-28) enables another decoder that in turn decodes the address lines A0 - A2 to generate yet another set of eight enabling lines that enable, typically, data bus I/O ports for the data transaction with the generator board, display/keyboard and the GPIB section. The read bank signals are utilized directly to enable I/O ports.

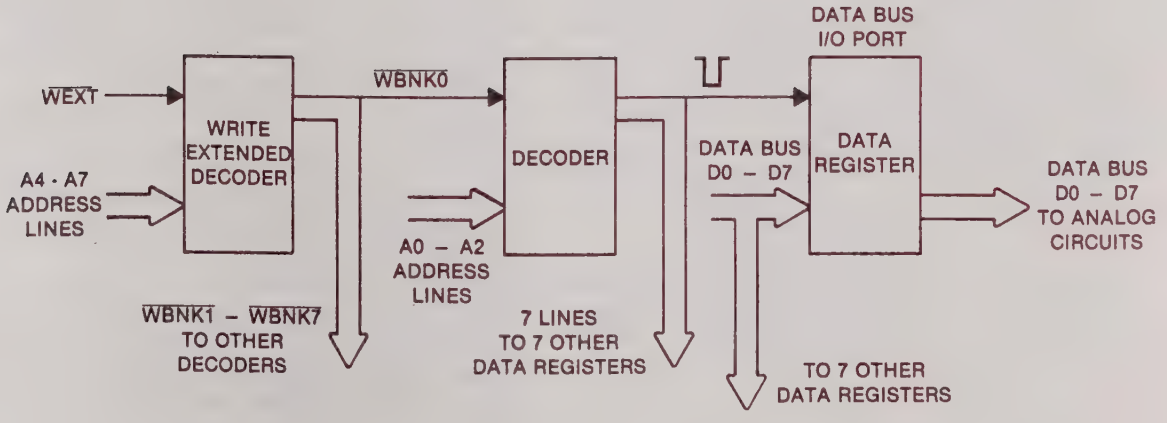

DATA BUS I/O PORT
WEXT
WRITE EXTENDED DECODER
WBNK0
DECODER
DATA BUS D0 – D7
DATA REGISTER
DATA BUS D0 – D7 TO ANALOG CIRCUITS
A4 - A7 ADDRESS LINES
A0 – A2 ADDRESS LINES
WBNK1 – WBNK7 TO OTHER DECODERS
7 LINES TO 7 OTHER DATA REGISTERS
TO 7 OTHER DATA REGISTERS

Figure 5-28. Typical Extended Bank Generated I/O Ports

Table 5-1 is a summary of programming data for the generator board. Each programmable parameter is listed with information identifying which register bits are programmed to control that parameter and short description of how the registers are programmed to get a desired output. The I/O port (register) numbers are composed of two digits. The first digit tells which write/bank line (0 = WBNK0, 1 = WBNK1) will be activated when the port is selected. The second digit selects which register in the group controlled by the activated write bank line will be updated.

Table 5-1. Summary of Generator Board Write Data

Parameter Name	I/O Port	Bits	Locations of IC Holding Information	Method or Programming Parameter (all values given in decimal numbers)
Sample Time:				The value field is programmed with a four digit BCD number to yield a sample time in hundreds of nanoseconds. The range field is programmed with a three bit binary number (between 0 and 6) which is the power of ten that is multiplied by the time selected by the value field to give the desired sample time. *Example:* For a desired sample of 12.34 ms, program 12 into upper 8 digits of value (binary 0001 0010) 34 into lower 8 digits of value (binary 0011 0100) 2 into range (binary 010) This selects 1,234 × 10^2 × 100 ns.
Range	00	1-3	15A	
Value (Upper 2 Digits)	01	0-7	13A	
Value (Lower 2 Digits)	02	0-7	14A	
Continuous/Triggered	00	4	15A	Single bit: 0 = continuous, 1 = triggered
Full/Partial Block	00	5	15A	Single bit: 0 = full block, 1 = partial block
Preset/Monitor	00	6	15A	Single bit: 0 = preset, 1 = monitor
Clock Internal/External	00	7	15A	Single bit: 0 = internal clock, 1 = external clock
Start Address	03	0-7	11A	This field is programmed with the desired start address, in the form of an 8 bit binary number ranging from 0 to 255.
Stop Address	04	0-7	10A	This field is programmed with 255 minus the desired stop address (which is the one's complement of the stop address) in the form of an 8 bit binary number ranging from 0 to 255. *Example:* To stop at address 63, 192 is programmed into this field.

Table 5-1. Summary of Generator Board Write Data (Continued)

Parameter Name	I/O Port	Bits	Locations of IC Holding Information	Method of Programming Parameter (all values given in decimal numbers)
Preset Length Counter:				This field is programmed with the binary one's complement of the 4 digit BCD value of the desired preset length. *Example:* To program a burst of 1593 blocks, program EA_{16} (binary 1110 1010) into the upper two digits and $6C_{16}$ (binary 0110 1100) into the lower two digits. The preset length may range from 0001 to 9999.
Upper Two Digits	05	0-7	7A	
Lower Two Digits	06	0-7	5A	
Cursor	07	0-7	4A	This field is programmed with 255 minus the desired cursor address (which is the one's complement of the cursor address) in the form of an 8 bit binary number ranging from 0 to 255. *Example:* To cause a cursor pulse at address 163, program 92.
Amplitude and Offset				The amplitude value is programmed with the absolute value of the desired amplitude, in units of 10 millivolts, in the form of a 10 bit binary number. The sign of the desired amplitude is programmed into the amplitude sign field (single binary bit: 0 = output normal, 1 = output inverted). The offset value is programmed with 512 minus the desired offset in units of 20 millivolts, also in the form of a 10 bit binary number. The attenuator field is programmed by setting the bit corresponding to the desired attenuation to one and setting all the others to zero. It is also legal to set all bits in this field to 0; this disconnects the output amplifier from the output BNC connector. Legal attenuator values are: 8 - no attenuation 4 - × 10 attenuation 2 - × 100 attenuation 1 - × 1000 attenuation 0 - output disconnected
Amplitude Value				
Upper 8 Bits	13	0-7	5G	
Lower 2 Bits	10	6-7	3G	
Amplitude Sign	10	5	3G	
Offset Value				
Upper 8 Bits	11	0-7	4G	
Lower 2 Bits	12	6-7	6G	
Attenuator	10	0-3	3G	

Table 5-1. Summary of Generator Board Write Data (Continued)

Parameter Name	I/O Port	Bits	Locations of IC Holding Information	Method of Programming Parameter (all values given in decimal numbers)
Amplitude and Offset (Continued)				The attenuator field controls the attenuation of both the amplitude and offset (refer to paragraph 3.13). *Example:* To produce a waveform with 153 mV of amplitude and −36 mV of offset, program 153 into amplitude field 0 into amplitude sign field 530 into offset field 4 into attenuator field
Smoothing Off/On	10	4		Single bit: 0 = smoothing on, 1 = smoothing off.
Function	12	0-4		This field selects which memory or combination of memories will be used to generate the output waveform. Legal codes are (in decimal): 0 - Sine wave ROM 1 - Triangle wave 2 - Square wave 3 - Ramp 4 - User-programmed PROM #1 5 - User-programmed PROM #2 6 - User-programmed PROM #3 7 - User-programmed PROM #4 8 - RAM block 1 9 - RAM block 2 10 - RAM block 3 11 - RAM block 4 20 - User-programmed PROM #1* 21 - User-programmed PROM #1 and #2* 22 - User-programmed PROM #1, #2 and #3* 23 - User-programmed PROM #1, #2, #3 and #4* 24 - RAM block 1* 25 - RAM blocks 1 and 2* 26 - RAM blocks 1, 2 and 3* 27 - RAM blocks 1, 2, 3 and 4* *Joined-together blocks

5.5 MICROPROCESSOR/GPIB INTERFACE

The microprocessor/GPIB interface allows the instrument to be remotely programmed by a minicomputer, calculator, etc., via the General Purpose Interface Bus (GPIB). The GPIB interface is an implementation of IEEE Standard 488-1975. It supports the following 488-1975 defined interface functions: Source Handshake (SH1), Acceptor Handshake (AH1), Talker (T6), Listener (L4), Service Request (SR1), Remote Local (RL2), Device Clear (DC1) and Device Trigger (DT1). This bus transfers messages in bit parallel and byte serial fashion. The bus has 16 signal lines, and they are:

8 Data lines (DIO1 through DIO8)
5 Control lines (ATN, IFC, SRQ, EOI and REN)
3 Handshake lines (NRFD, NDAC and DAV)

These lines are defined in paragraph 3.16, as is operation with the GPIB.

The microprocessor/GPIB interface does the following three functions:

1. Detects the My Listen Address (MLA) and My Talk Address (MTA).

2. Does the proper listen handshake when either attention (ATN) is true, or the listen latch is set, and transfers messages when the talk latch is set.

3. Provides isolation through optical couplers.

In order to reduce the number of opto-isolators, the messages are transferred in bit serial fashion through two Universal Asynchronous Receiver/Transmitters (UART). (See figure 5-29.) All 16 GPIB lines are buffered and terminated through bus transceivers. The UART and status outputs are connected to the microprocessor data line via tri-state buffers.

The operation of the UART is fairly simple. Each UART consists of two independent sections called receiver and transmitter, and both of them may operate simultaneously. The UARTs are primarily used to convert parallel information into serial and serial information into parallel. The receiver receives its information in serial and converts it into an 8 bit parallel byte, whereas the transmitter converts an 8 bit parallel byte into bit serial output. The transfer rate of the serial output is 16 times the clock frequency of the UART. Here the UART clock frequency is set at 1.25 MHz.

The interface completely insulates the microprocessor from GPIB and hence the microprocessor is relieved from the GPIB transactions. The microprocessor constantly monitors the status outputs from the interface and takes actions according to them. There are six status bits tied to the microprocessor data bus: Data Ready, GPIB Busy, End, Remote, Talk and Listen.

5.5.1 Data Ready

The Data Ready bit informs the microprocessor that the UART has received valid data from the GPIB. Only when this bit is true will the microprocessor read the byte from the UART.

5.5.2 GPIB Busy

The GPIB Busy bit is used during the talk mode to find out whether GPIB has accepted the data byte sent through the UART. Any time the microprocessor wants to send a byte via GPIB, first it checks that the Talk status bit is true and then it checks that GPIB Busy status bit is false. If the GPIB Busy status is false, then the microprocessor will load a byte into the UART and cause the GPIB Busy signal to go high (true). This prevents the microprocessor from loading any more bytes into the UART. The byte loaded into the UART is transmitted serially across the opto-coupler to the GPIB side of the UART. When all the 8 bits of the byte are present, the data valid (DAV) line is set low. When the listener on the GPIB senses the DAV line is low, he accepts the byte by raising the data accepted (NDAC) signal high. The NDAC signal is received and causes the GPIB Busy signal to go low (false). Once the GPIB Busy signal goes low, the microprocessor can transmit another byte in the same manner.

5.5.3 End

The End bit is monitored by the microprocessor any time it reads a byte from the UART. If this bit is true, then the microprocessor assumes that it has received the last byte of the message sequence and treats it as a terminating character.

5.5.4 Remote

The Remote bit indicates to the microprocessor whether the Arb is in remote control or local control.

5.5.5 Talk

The Talk bit will be set any time the Arb receives its assigned talk address. When the microprocessor

senses this bit as true, it prepares to send the data bytes through the UART.

5.5.6 Listen

The Listen bit will be set any time the Arb receives its assigned listen address. When the microprocessor senses this bit as true, it prepares to receive the data bytes through the UART.

5.5.7 Service Request

Service Request (SRQ) is a bit sent by the microprocessor to the GPIB when it needs attention.

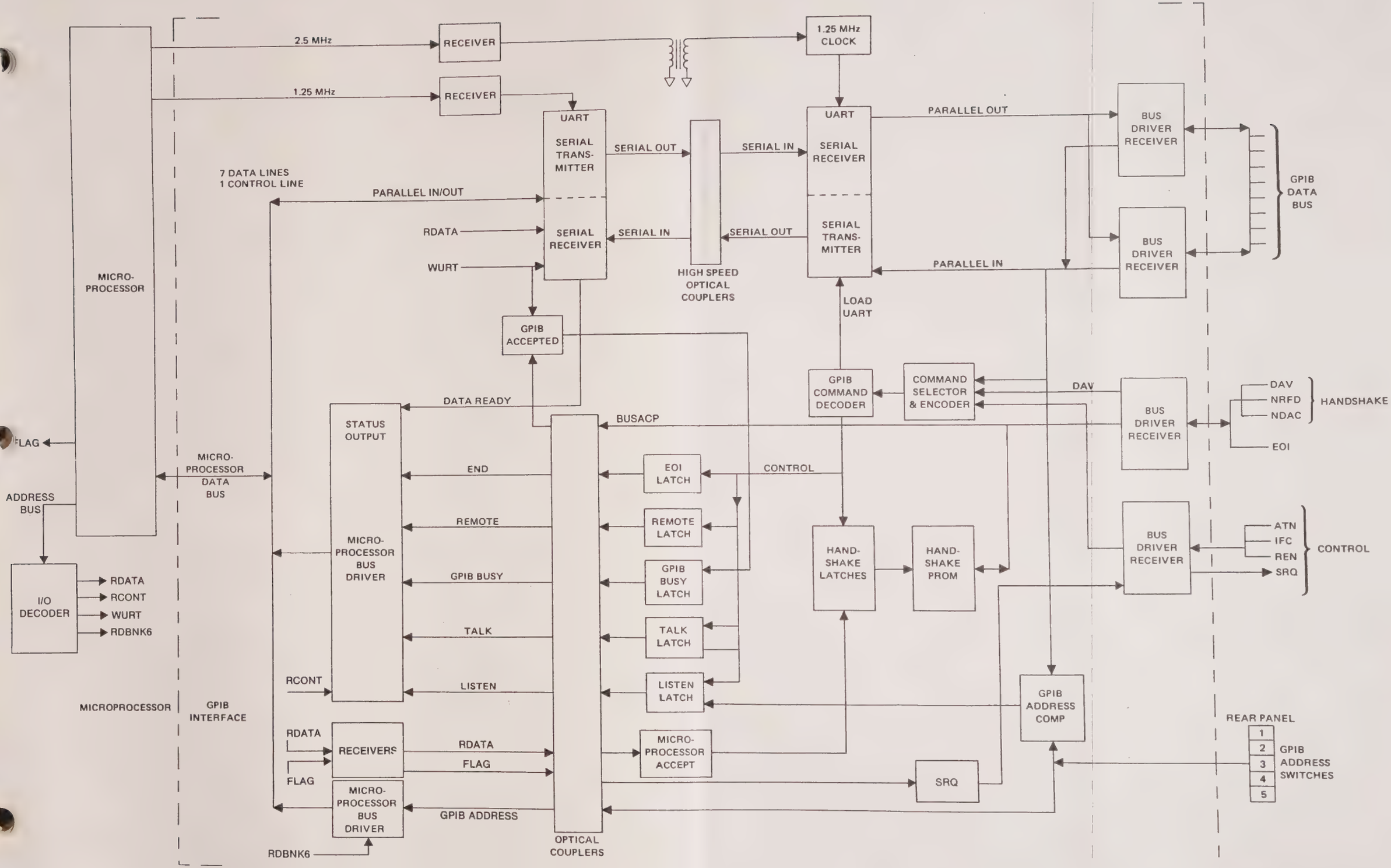


Figure 5-29.
GPIB/Microprocessor Interface Block Diagram

SECTION 6
TROUBLESHOOTING

6.1 INTRODUCTION

Faults may be isolated to four major assemblies of the Arb: the power supply group containing the rear panel, heatsink and power supply board; the front panel and display board assembly; the microprocessor and GPIB interface board; and the arbitrary generator board (see figure 5-1). Familiarize yourself with the Arb by reviewing the operating procedure in this manual, as well as the circuit descriptions. Successful fault isolation depends upon a thorough knowledge of the correct instrument operation.

Fault isolation is discussed in the following paragraphs in terms of the four major assemblies. The locations of boards and interconnections being discussed are shown in the Chassis Assembly (0102-00-0666) in Section 7 of this manual. Once a fault is isolated, refer to the schematics, assemblies and parts lists of the various subassemblies that follow in Section 7.

6.2 POWER SUPPLY

In case the Arb is malfunctioning, power supply voltages are always the first thing to be checked. The power supply produces +15V, −15V, +5V (for logic) and ISO +5V (for GPIB interface).

The display board requires the +5V logic supply and +15V (used only for the sounder). The generator board uses +15V, −15V and +5V logic supplies. The microprocessor uses +5V logic and the GPIB section requires both +5V logic and ISO +5V.

The +15V and −15V supplies can be measured at R79 and R82, respectively, on the generator board (-0644). The +5V logic supply can be measured from TP7 (+) to TP8 (COM) on the microprocessor/GPIB board (-0660). Likewise, the ISO +5V supply may be measured from TP9 (+) to TP10 (COM).

The +15V supply is also the reference for the −15V and +5V logic supplies and should be verified first when checking supplies. When encountering a problem in any of the supplies, first check their unregulated inputs. Check for +22 Vdc across C15 on the power supply board (-0659), −22 Vdc across C25, +10 Vdc across C35 and +10 Vdc across C1 on the rear panel (-0667). Incorrect or missing readings at all of these inputs indicates a problem in the line voltage, line voltage selector, power switch (or wiring), fuse, thermal cut-off (on heatsink), transformer or P1 wiring from rear panel to power supply board. A bad reading in any one could be its associated rectifiers (-0659), or if slightly low, an excessive current drawn from the input. The isolated (ISO) supply is not common to the other supplies, so it must be measured with respect to its own common (COM).

CAUTION

Make sure power is off when connecting and removing connectors.

The +15V supply receives +22V unregulated from C15. It is dependent upon the −15V supply only for the minus supply at U3 pin 4. It has current fold-back protection from the action of R17 and Q9, so a low +15V may be caused by the load and may be isolated to the generator or display boards by removing P4 or P6 from the power supply board. Once verified that the problem is current fold-back, it is more often advantageous to reconnect the load and isolate the problem through locating heating components. This method would not be advisable with the +5V logic supply, which supplies a much higher current. The +15V supply regulates by U3 pin 6 controlling the current through pass transistor Q7 (on the heatsink), so that the voltage at pin 3 equals the +6.4V zener reference at pin 2. Q9 is off, except in current fold-back. A failure most often produces a high, nonregulated output and usually is shorted or open transistors Q7 - Q10.

The −15V regulator operation is similar to the +15V regulator discussion, except that it is referenced to the +15V supply. When normal, it produces a negative voltage equal in magnitude to the +15V. A failure is usually Q11 - Q14. It receives −22V unregulated from C25.

The +5V logic supply receives +10V unregulated from C1 aluminum electrolytic on the rear panel. The heatsink contains R1 and Q1 current limiting elements, Q2 pass transistor, and CR24 overvoltage protection SCR. The supply regulates through U1 pin 6 controlling the current through Q2, so that pin 2 equals the +3V reference at pin 3 derived from the +15V supply. Excessive current to the load is detected across R1 (7A = 0.7V), turning on Q1 and turning off Q2. An overvoltage of approximately +5.5V or a transient is detected by U2 SCR trigger which fires CR24, shunting the output to approximately +1V. The SCR may be reset by turning the power off, allowing a few seconds to discharge C1, then turning the power on. The SCR will be turned on by turning the power off, then on, too rapidly; by turning it on without a substantial load on the +5V logic supply; or by a high +5V or +15V regulator. Because of these difficulties, it is best to troubleshoot the +5V logic supply in the following manner.

CAUTION

Make sure power is off when connecting and removing connectors.

Remove P4, P5 and P6 from the regulator board and connect a 1 to 2 ohm, 25 watt or greater resistive load across C9 on the regulator. If the supplies function, there is a loading problem with one of the other boards. Leave the resistive load in and try connecting P5 and P6 to isolate the problem to microprocessor or display boards. If the supply is still regulating, remove the resistive load and connect P4, isolating the problem to the generator board. Do not leave the supply on and loaded down for more than a few seconds at a time or board damage may result.

If the regulator does not operate with P4, P5 and P6 removed and the resistive load in, check the +15V, unregulated input at C1 and +3V at U1 pin 3. Generally, the regulator will fail by trying to go too high, turning on the SCR, which drops the output to +1V. U1 pin 2 should then be less than 1V and the output at pin 6 will saturate high. The problem should be Q1, Q2 and Q3.

The ISO +5V supply receives +10V unregulated from C35. The regulator is a 7805 (Q18 on heatsink) which has internal current limiting and thermal shutdown. Removing P5 from the regulator board isolates the supply from its load.

6.3 FRONT PANEL DISPLAY

Display status is the first and most obvious indication of a fault. The display, keyboard and microprocessor have such an intimate relationship that it can be difficult to isolate a problem. Often, observing the status of the generator via its outputs can be a means of determining whether the machine software is awake, since the generator and display both respond to the contents of the microprocessor's working RAM buffers. Also, the GPIB interface may be helpful as an isolation aid by checking whether the unit responds to functions deficient on the front panel. Refer to table 6-1 for troubleshooting hints and paragraph 5.3 for circuit description.

Table 6-1. Front Panel Troubleshooting

Symptom	Further Observation	Probable Cause
1. When turned on, display flashes random data for an instant, then goes dark.		1. +5V logic supply in overvoltage protection mode. 2. +15V supply in current overload mode.
2. Display reads nonsense; keyboard dead.	Microprocessor is probably not properly initialized. To verify, check ARB OUT (HI) BNC for 1V pk sine at 195 Hz which should also be missing. If ARB OUT (HI) is good, go to symptom 3.	Go to paragraph 6.4.

Table 6-1. Front Panel Troubleshooting (Continued)

Symptom	Further Observation	Probable Cause
3. Display reads nonsense; keyboard may be dead.		Marginal power supply.
	1. Display showing only specific segments in specific digits even when LAMP TEST is pressed.	1. Display clock U30. 2. Clock dividers and multiplexers U18, U19, U10, U11.
	2. Display missing only specific segments or digits, even when LAMP TEST pressed.	1. Bad LED or display. 2. Bad segment or digit driver. 3. Bad multiplexers.
	3. If turn-on nonsense persists, even if microprocessor initializes display data registers and/or key-read register may not be getting clocked.	1. Read/write decoders U20C and U20D on microprocessor. 2. I/O decoder UID on microprocessor. 3. U27, U31, U32 on display.
	4. Incorrect label and units alphas displayed.	1. Bad U23. 2. Data bus hung up outside microprocessor buffers. 3. Bad U12 or LADs and UADs hung up on display board.
	5. Incorrect numerals displayed.	1. Address or data bus hung up outside microprocessor buffers. 2. U16, U17, U31 on display.
	6. LED not lighting.	1. Bad LED. 2. Related data register.
	7. LED not extinguishing.	1. Related data register bad. 2. Related data register getting a CLK input incorrectly.
4. Display flickering.		1. Clock U30. 2. Counter U19 or U10.
5. Keyboard bad.	No keys work.	1. Read extended decoder U20D or I/O decoder U11K on microprocessor. 2. U26, U27, U28, U29 on display. 3. Connector P28 on keyboard.
6. Certain keys do not work.	1. Inoperative keys can be related to a particular column on row in the key matrix.	1. Column not being strobed by U28. 2. Open circuit in connector P28. 3. Bad keyboard.
	2. Inoperative keys can be related by a certain binary digit in columns decode.	1. U26 not counting correctly. 2. U27 not transmitting a bit.
	3. Inoperative keys can be related by a certain binary digit in rows decode.	1. U27 not transmitting a bit. 2. U29 bad or hung up.

Table 6-1. Front Panel Troubleshooting (Continued)

Symptom	Further Observation	Probable Cause
	4. Bad key or keys cannot be related.	Bad keyboard.
7. Certain keys produce incorrect response.	A column or row loaded down or two sections shorted together will appear to U29 priority encoder as multiple keystrokes and it will encode the highest order key.	1. Bad keyboard. 2. Loaded down row or missing pull-up resistor. 3. U27 not transmitting all bits correctly, but binary relationship was not obvious.
8. Improper display of hold LED, length counter, memory address or memory data.		1. Related circuits in generator (refer to paragraph 6.6). 2. Read extended decoder U20D on microprocessor.
9. Poor acoustic feedback.	1. No sound.	1. ♪ Key accidentally pressed. 2. Transducer has obstruction or broken wires. 3. U32, U15, Q1, Q2. 4. +15V missing to display.
	2. Low volume and/or poor tone.	1. Transducer not centered in holder or wire pinched in holder. 2. Q1, Q2. 3. Microprocessor clock marginal or counter U19 D1 on microprocessor board.

6.4 MICROPROCESSOR

The GPIB interface portion of the microprocessor/GPIB board is treated separately in paragraph 6.5. Figure 6-1 gives a microprocessor block diagram and major flow of the GPIB for clarity. The basic microprocessor hardware can be tested without special equipment as follows.

Force a no-operation (NOP) condition into the 2650 microprocessor with a "C0" on the data bus. Do this by removing the jumper at J1, placing the jumper at J2, and removing the shunt at U11A, which disconnects the memory data bus from the microprocessor. Turn the unit on and check the +5V logic supply at TP7 (+) and TP8 (COM). Check the 1.25 MHz clock (800 ns) at U12D pin 38; check for a low at pins 15, 16, 25 and 36; check for a high at pins 1, 17 and 37; and check for a C0 (1100 0000) at pins 26 through 33. If a C0 is not present, there may be a failure in U12D, U16D or U10A and the affected device could be hot. With a C0, the microprocessor address bus at pins 14 through 3 should be running like a binary counter. The buffered addresses at U13C and U14C should also be running. P10 and P11 may be used to isolate hung-up buffered address lines to the generator or display. The memory decoder U17C should now be producing sequential low pulses to enable the memory. Sync on $\overline{PR0}$ at U17C pin 1 and check pins 19 and 20 of EROMs U12A, U13A and U15C for enable pulses.

If the basic microprocessor is functional, return the jumper to J1 and reinstall shunt U11A. If the microprocessor is not responding (via the display or generator output) when the unit is turned on, try removing P10 and see if the generator works without the display. Initial conditions for the generator would be indicated by a 1V peak, 195 Hz sine wave present at the ARB OUT (HI) BNC. If the problem is found to be due to generator or display being connected, try to locate hung-up address or data lines on those boards. If none of the above results in a responding condition, either the microprocessor has hung-up memory data lines or it is actually responding, but not sending, control inputs to the data registers on the other boards.

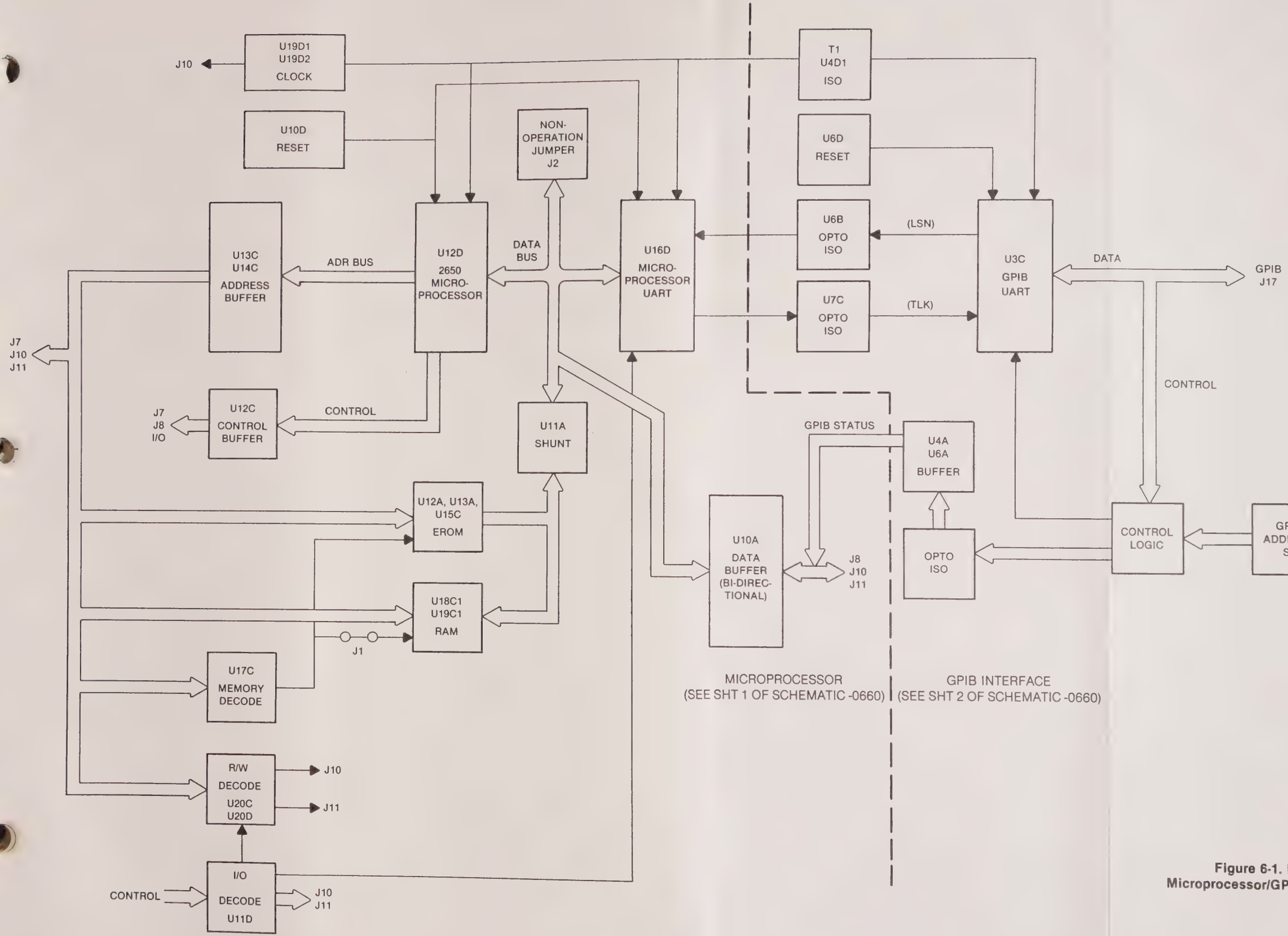


Figure 6-1. Microprocessor and Microprocessor/GPIB Interface Block Diagram

If there is activity on all eight data lines, the microprocessor/software should be in its read routines and have finished writing out the initial conditions. Go to table 6-2 for troubleshooting hints.

CAUTION

CMOS/MOS devices may be damaged by static charges. Discharge yourself prior to handling EROMs, RAMs, UARTs and microprocessors. Handle the devices by their bodies only and place on conductive material when not in use.

If data lines appear hung up, remove U10A and U16D to isolate the problem to the memory. J1 may also be pulled to disable the RAM memory. EROM memories are on sockets, so the problem should be isolated to a single device.

If nothing appears to be wrong with the microprocessor data bus or any of its read/write outputs, but the unit does not respond, it could have an EROM failure, which just sends a routine to a dead end. It may even set most or all of the initial conditions, but ignore the keyboard, or even respond to keys until a particular key is pressed. In this case, the microprocessor board should be sent back to Wavetek, unless a spare EROM set is available.

6.5 GPIB INTERFACE

Refer to figure 6-1 and to the circuit description in paragraph 5.5. It is also valuable to have literature available on the GPIB bus itself, especially command structure and handshaking sequence. Before running any of the following tests, verify the following:

1. The unit operates properly, except for the GPIB.
2. There is +5V ISO at TP9 (+) to TP10 (COM) on the microprocessor board.
3. There is a 1.25 MHz clock at U16D (LOGIC) and U3C (ISO) pins 17 and 40. Their pins 21 are low.
4. $\overline{\text{RCONT}}$ at U6A pins 1 and 19 is running.
5. Unit displays its own GPIB address. If not, check opto-isolators (U1A3, U2A2, U1A2, U2A1 and U1A1), buffer U4A and that $\overline{\text{RBNK6}}$ is present when GPIB ADRS key is pushed.

6.5.1 Test 1 — Bus Hung Up

1. Disconnect GPIB cable and turn the Arb on. Check all 16 GPIB lines for highs at J17 and at the received outputs (R63) from 3446 receiver/transmitters.
2. Connect an external TTL signal with a period of approximately 1 ms to DAV at TP5 referenced to ISO COM. If possible, use a negative pulse with approximately 10% duty cycle.
3. Connect a jumper between TP6 (ATN) and TP10 (ISO COM).
4. Set GPIB address switch so that display reads address 0.
5. Display RDAV at U1B pin 1 on channel 1 of oscilloscope and sync to it. Use channel 2 to observe other signals. Check for a low RATN at U2B pin 1.
6. Check U5C pin 1 (EQUAL) for a positive pulse.
7. Check U7B pin 15 for a negative pulse delayed approximately 500 ns from RDAV.
8. Connect REN at U2B pin 10 to ISO COM and check for a high at U8B pin 1.
9. Momentarily ground U8B pin 3 and note that both REM and LIS LED's come on.
10. Check handshake lines NRFD (J17 pin 7 for a negative pulse) and NDAC (J17 pin 8 for a positive pulse).

Table 6-2. Microprocessor Troubleshooting

Symptom	Further Observation	Probable Cause
1. Unit not responding, displays random data after turn-on.	Power supplies OK.	Complete the NOP test detailed in paragraph 6.4.

Table 6-2. Microprocessor Troubleshooting (Continued)

Symptom	Further Observation	Probable Cause
2. NOP test OK; data lines are running free; unit still does not respond.	1. Data registers on generator board and display board may not be getting loaded with initial conditions set up in RAM memory. Refer to table 6-3.	1. Missing WE pulse U11C, U18D, U12C, U13C, U12D or no continuity from microprocessor to other-boards. 2. Missing $\overline{\text{WBNK}}$ pulses U20C, U11D, U17C, U12C, U12D or no continuity. from microprocessor to other boards.
	2. RAM memory not being loaded.	1. U18C1 or U19C1. 2. $\overline{\text{RAM}}$ missing. 3. $\overline{\text{MOP}}$ missing. 4. EROMs U12A, U13A, U15C.
	3. EROM firmware not responding. (Address stops at dead end).	U12A, U13A, U15C.
3. Unit displays initial conditions, but does not accept inputs from keyboard or GPIB.		U11D circuitry; no $\overline{\text{RDATA}}$ or $\overline{\text{REXT}}$.
4. Unit accepts data over GPIB, but not keyboard.	1. No $\overline{\text{RBNK4}}$.	U20D circuitry.
	2. $\overline{\text{RBNK4}}$ OK.	1. No continuity from microprocessor to display U27 pins 1, 19. 2. Display board problem; go to table 6-1, symptom 5.
5. Unit accepts data from keyboard, but not over GPIB.	1. $\overline{\text{R DATA}}$ bad.	U11D circuitry.
	2. $\overline{\text{R DATA}}$ OK.	1. URTDA U16D pin 19. 2. $\overline{\text{WURT}}$ hung high. 3. Go to table 6-4.
6. Unit does not transmit data over GPIB.		1. $\overline{\text{WURT}}$ BAD. 2. Go to table 6-4.
7. Data not reaching generator.		1. $\overline{\text{WBNK0}}$ or $\overline{\text{WBNK1}}$ at U20C. 2. WE ANALOG at U11C, U12C. 3. No continuity above signals or an address or data line to generator. 4. Generator problem; go to table 6-5.
8. Data not being read from generator.		1. $\overline{\text{RBNK0}}$ through $\overline{\text{RBNK3}}$ at U20D. 2. No continuity with these lines to generator. 3. Go to table 6-5.

11. Momentarily short U5A pin 1 to U7B pin 4 and note that LIS LED goes out and U4D2 pin 5 goes high.

12. Remove jumper from TP6 to TP10 and note that TLK LED comes on.

13. Momentarily short U2B pin 6 to TP10 and note REM and TLK LED's go out.

Any failures in this test should be straightforward to troubleshoot, since the GPIB interface is being forced to run even if it would not handshake with a GPIB controller.

Table 6-3. Summary of Generator Board Programming Data

	Port	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	IC Location
WE	00	CLOCK INT/EXT	MNTR/ PRST	FULL/ PART	TRIG	SAMPLE TIME RANGE				15A
	01	SAMPLE TIME (MSD)				SAMPLE TIME (DIG2)				13A
	02	SAMPLE TIME (DIG3)				SAMPLE TIME (LSD)				14A
	03	START ADDRESS								11A
	04	STOP ADDRESS								10A
	05	PRESET LENGTH (MSD)				PRESET LENGTH (DIG2)				7A
	06	PRESET LENGTH (DIG3)				PRESET LENGTH (LSD)				5A
	07	CURSOR								4A
	10	AMPLITUDE LS 2 BITS		AMPL +/–	SMOOTH/	0 dB	20 dB	40 dB	60 dB	3G
	11	OFFSET								4G
	12	OFFSET LS 2 BITS		5 NOT USED	FUNCTION					6G
	13	AMPLITUDE								5G
	14	HOLD PULSE								7G/9C
	15	TRIGGER PULSE								7G/15C
	16	RESTART PULSE								7G/14C
RE	2X	CYCLE COUNTER MSB								8A
	3X	CYCL COUNTER LSB								6A
	0X	HOLD ADDRESS								12A
	1X	RAMP TO ZERO/COMMAND (BIT 1) AND HOLD BIT (BIT 0) FROM EXTERNAL BNC								4C

Table 6-4. GPIB Troubleshooting

Symptom	Further Observation	Probable Cause
1. GPIB does not function.	1. Neither TLK or LSN will come on.	GPIB address switch does not match address sent by controller.
	2. DAV is not running, indicating GPIB is hung up.	Go to test 1, paragraph 6.5.1.
	3. Unit passes test 1, but gets no REM and LSN LED when used with a GPIB controller.	Go to test 2, paragraph 6.5.2.
	4. Unit gets REM and LSN, but passes no data.	Go to test 3, paragraph 6.5.3.
2. GPIB listens, but does not talk.	1. No TLK LED; passes test 1.	1. Controller not sending proper talk address; refer to paragraph 2.2.4. 2. Go to test 4, paragraph 6.5.4.
	2. No data (good or bad) being sent from Arb.	1. Read paragraph 3.16.4 on talk status and terminating character. For example, an R3-10 would set up the Arb to send last programmed value to an HP 9825. 2. Go to test 5, paragraph 6.5.5.
3. GPIB produces errors when Arb listening.	1. Errors in bit values.	U6B, U3C, U16D, U1C, U2C; 1.25 MHz clock noisy at either UART.
	2. Missing bytes.	U7D2, U5D2.
4. GPIB produces errors when Arb talking, but not in listening.	1. Errors in bit values.	U7C.
	2. Missing bytes or nonsensical bytes.	U8D, U9A or handshake (go to test 5, paragraph 6.5.5.).

6.5.2 Test 2 — Handshake

1. Press GPIB address key and set up a GPIB controller to send that talk address continuously. For example, with an HP 9825A, send "wrt 701" in a loop for Arb address "1".

2. Verify that REM and LSN are on. If REM and LSN are not on, study figure 6-2 and the following discussion.

Command selector U4B is a 256X4 PROM, programmed to detect the GPIB commands and encode them into a 3 bit binary output as follows:

DATA BYTE	000
TALK ADDRESS	001
UNLISTEN	010
LISTEN ADDRESS	011
GO TO LOCAL	100
ADDRESSED CMD	101
UNIVERSAL CMD	110
DON'T CARE	111

The encoded commands are fed to another PROM (U7B) command decoder. The $\overline{\text{LSNADD}}$ output is generated any time there is a listen address on the bus. The address comparator produces an EQUAL output each time the bottom five data lines match the

setting of S1. The combination of $\overline{\text{LSNADD}}$ and EQUAL produce $\overline{\text{MLA}}$, my listen address, which is a low following DAV whenever the Arb's own listen address is being sent. $\overline{\text{MLA}}$ sets the REM and LSN flip-flops (U8B).

If DAV is running, $\overline{\text{MLA}}$ should be produced, and REM and LSN LEDs should be on. Test 1 checks most of the handshake hardware, but the bus may hang, depending upon the nature of the problem and on the type of controller used. Handshake PROM U5A should be enabled (pin 15 low) and should initialize with TNRFD and TNDAC low (refer to NRFD and NDAC, figure 6-3). Both being high is an error condition with most GPIB controllers, and one or the other being hung high can hang up the bus; thus, ATN and DAV would not be running. A high NRFD or NDAC may be pulled low at U5A pin 1 or 2 to clear the bus and aid troubleshooting.

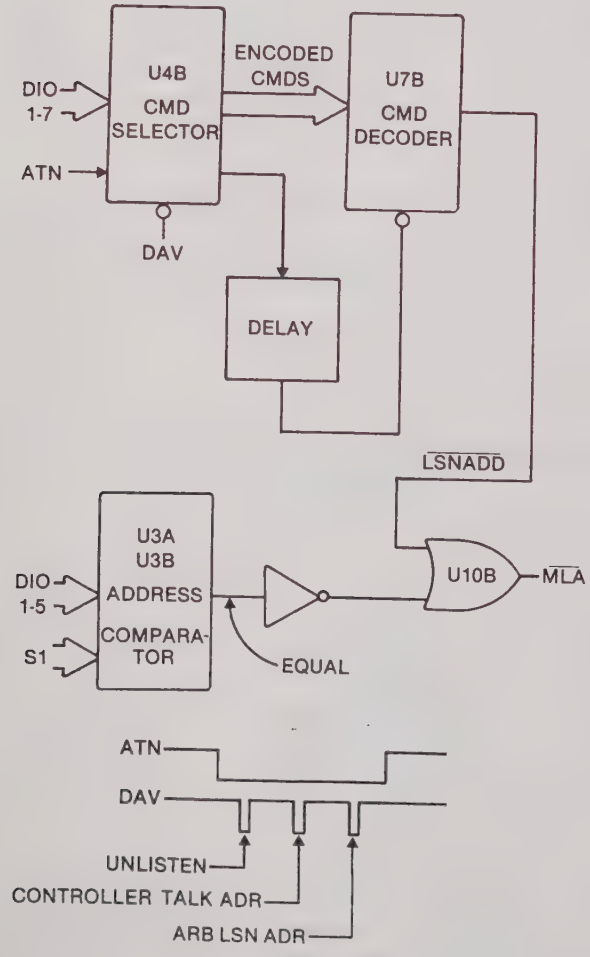


Figure 6-2. MLA Diagram

Figure 6-3 and the following steps of the handshake process apply only to one controller and one listener on the bus.

1. Controller has data valid (DAV) high (false) and puts a byte of data on the bus. After a settling time, it is ready to set DAV low when listener indicates it is ready for data (NRFD high).
2. Listener has initialized both NRFD and NDAC low.
3. Listener sets NRFD high indicating it is ready to accept data.
4. Controller responds by setting DAV low (data valid).
5. Listener sets NRFD low.
6. Listener accepts data byte.
7. Listener sets data accepted (NDAC high) indicating data byte has been accepted.
8. Controller sets DAV high and places second data byte on bus.
9. Listener sets NDAC low.
10. Listener sets NRFD high when ready for next byte.
11. Controller sets DAV low.
12. Listener sets NRFD low.
13. Listener accepts second byte.

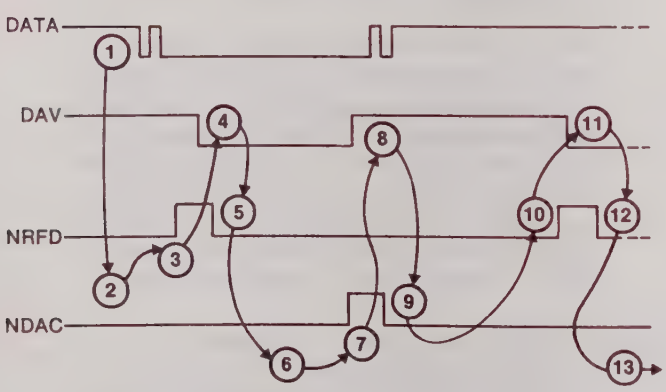
The handshake in command mode (talk and listen address) does not send data over the UART to the microprocessor, but is processed immediately. When command bytes are sent, $\overline{\text{STRB2}}$ at U7B pin 2 goes low and sets flip-flop U5D1. This produces the signal $\overline{\text{DAVY}}$ which completes the handshake process at U5A.

6.5.3 Test 3 — Listen Mode

1. When a data byte is transmitted, U7B pin 1 $\overline{\text{STRB1}}$ must go low to load the byte into UART U3C. $\overline{\text{STRB1}}$ produces a pulse called CKDAV via delay circuit U5D2 and U9C. CKDAV goes low for approximately 5 microseconds and during this time the data byte is loaded into UART U3C from $\overline{\text{LDU}}$ at U5D2 pin 9. When CKDAV goes high, it clocks U5D1 and produces $\overline{\text{DAVY}}$ to complete the handshake. Check that handshak-

ing is taking place and the LDU is present at U3C pin 23.

2. Verify the presence of the signals referred to in the following discussion. In listen data mode, synchronization is achieved by the LISTNBUSY HOLD flip-flop U5D2. $\overline{\text{LDU}}$ loads a byte and sets LIS BUSY which locks up the CMD DECODER U7B and prevents it from producing $\overline{\text{STRB1}}$ outputs and thus completing handshake. The byte loaded into U3C is transmitted serially, via opto-coupler U6B, to the microprocessor UART U16D. This UART converts the serial data back into 8 bit parallel data. When the byte is assembled and available, the UART sets URTDA at pin 19 which goes to the GPIB status buffer U6A to be read by the microprocessor with a $\overline{\text{RCONT}}$ pulse. The microprocessor reads the data byte from the UART by generating a $\overline{\text{RDATA}}$ pulse. The $\overline{\text{RDATA}}$ pulse also goes through opto-coupler U7D2 to generate the μPACP pulse. This pulse closes the loop by clocking U5D2 and resets LISBUSY to low. Then the CMD DECODER is allowed to handshake the next byte by issuing a $\overline{\text{STRB1}}$ or STRB2. Problems in this area are generally the LIS BUSY flip-flop U5D2, optical couplers U6B or U7D2, or the signals $\overline{\text{RDATA}}$ and μPACP.



NOTE: REN and ATN are low.

Figure 6-3. Handshake

6.5.4 Test 4 — Talk Address

Verify the presence of signals referred to in the following discussion.

Read Test 2, as the listen address and talk address are processed in much the same way. The primary difference between the two is the way the talk flip-flop U4D2 is set. It is clocked by $\overline{\text{TLKADD}}$ from the CMD DECODER U7B every time a talk address is put on the bus, but the D input is EQUAL right off the address comparator. This allows the TALK flip-flop to clear itself whenever someone else's talk address is on the bus.

When the Arb is being addressed as a talker, it is actually still listening and handshaking in command mode as it was when addressed to listen. $\overline{\text{STRB2}}$ will complete the handshaking. When TALK is set, a high RATN (controller drops control of bus) at U6C pin 13 will produce a low $\mu\overline{\text{PTALK}}$ which is transferred via opto-coupler U8A2 to status buffer U6A and to the microprocessor when $\overline{\text{RCONT}}$ pulse goes low. When talk is set, it should also clear the LISTEN flip-flop.

6.5.5 Test 5 — Talk Mode

Check that U5A pin 15 is low. Write a looping program using talk status R3 where the controller makes the Arb a listener, puts some data in the display, then makes itself a listener, and reads the display data. Read the following circuit description and check the signals $\overline{\text{WURT}}$, GPIBUSY, RNRFD, RNDAC, TDAV, DA, DRDY, $\overline{\text{ACCEPT}}$, ACCEPT and BUSACP. Check opto-couplers U8D and U7C.

In talk mode the handshake PROM U5A will control the DAV in response to RNRFD and RNDAC from the acceptor device and DRDY at pin 3. U5A is enabled by $\overline{\text{TALK}}$ at U9B.

When the controller releases ATN, the microprocessor is informed that it is a talker and it places a byte on the data bus determined by the TLK STATUS (refer to paragraph 3.2.1, item 4). A string of bytes followed by a terminating character and EOI will be sent and then the controller will reset the ATN and take control of the bus.

The microprocessor loads the byte into microprocessor UART U16D by producing an approximate 1.1 microsecond negative $\overline{\text{WURT}}$ pulse. $\overline{\text{WURT}}$ also sets GPIB BUSY flip-flop U9A putting a GPIBUSY on the status buffer U6A and preventing the microprocessor from sending another byte. The byte is transmitted serially through opto-coupler U7C and reconstructed into parallel 8 bits by the GPIB UART, U3C. When U3C is loaded, it sets DA (Data Available pin 19) high. This signal is delayed and becomes DRDY to handshake PROM U5A. When RNRFD from the acceptor is high, the handshake PROM transmits a low DAV. When the acceptor sets NRFD low and

NDAC high, the handshake PROM releases DAV. The high RNDAC is also sent to clock U10C and produces a widened ACCEPT and $\overline{\text{ACCEPT}}$ pulse. $\overline{\text{ACCEPT}}$ clears the DRDY flip-flop U10C, the GPIB UART, and the EOI flip-flop U4D2 in case this was the termination byte when the 8th bit is used to set EOI. ACCEPT is sent through opto-coupler U8D and becomes the BUSACP clock to reset the GPIBUSY flip-flop U9A. This allows the microprocessor to put another byte on the UARTs. In this manner, synchronization is achieved between the Arb microprocessor and the acceptor device.

6.6 GENERATOR

The generator section troubleshooting is summarized in table 6-5. A functional test of the generator follows.

1. Turn unit on or reset if already on. Check REF OUT BNC for a 10 MHz TTL signal. If missing, check for a low $\overline{\text{INT}}$/EXT at U15A pin 19 and U17B pins 1 and 10, 10 MHz at U17B pin 13 and U16D pin 10 and coax to J20.

2. Program sample time to 2E-7 and check TP2 for a 200 ns (5 MHz) signal. If not present, verify U14C pin 10 is high. If pin 10 is low, there is a problem in the trigger logic or "TRIG" at U15C pin 3 is not low (false). If signal is not present and pin 10 is high, there is a problem in the sample time generator; or sample time data of a BCD "0002" is not being sent from data registers U13A and U14A; or U16A is not clocking data registers; or WE ANALOG, $\overline{\text{WBNK0}}$, AD0, AD1 or AD2 are missing.

3. Program sample times 4E-7, 8E-7, 1E-6, 2E-6, 4E-6, 8E-6, 1E-5, 2E-5, 4E-5, 8E-5, 1E-4, 2E-4, 4E-4 and 8E-4 and check for proper sample times at TP2 in all cases.

4. Press RESET key and check TP5 for 200 ns signal. If missing, check U18E and U16C trigger logic.

5. Check U15E pins 2, 4 and 5 for 200 ns signal. If pin 5 signal is missing or incorrect, check A,B,C inputs for a 010 or a bad U15E. Check U15E pins 1 and 3 for a 2 μs signal, pin 15 for 20 μs, pin 14 for 200 μs and pin 13 for 2 ms. Any missing signals would be U17C or U17E. Ensure their clear inputs are low (2 and 14).

6. Check TP6 for a 20 μs pulse. Wrong or missing signal would indicate a problem in the interpolation counter. The interpolation counter is set to count from 156_2 to 255_2 continuously. Check U15F and U14F Q outputs to ensure they are all running properly or a problem will show up in smoothing. Ensure that U15D pins 3, 5, 8 and 12 are low. (This logic is used when going from CONT to TRIG mode, a series of $\overline{\text{RESTART}}$ pulses clear the range counters, load the interpolator and address counters and advance waveform registers A and B so that the output is sitting at the start point of the selected function).

7. Check Q outputs U11B and U12B address counter for a 256_2 count. If missing, check for pins 9 high.

8. Check U10C pin 12 for a 20 μs negative pulse occurring at a 195.31 Hz rate. If missing, check $\overline{\text{END}}$ data for low-true 255_2 and U8B and U10B.

9. Check sync output for 20 μs positive pulse at 195.31 Hz.

10. Check cursor output for 20 μs positive pulse at 195.31 Hz which moves in time with respect to sync as address X is changed on front panel. Missing or incorrectly placed cursor may be a problem in cursor output circuit or $\overline{\text{CUR}}$ low-true binary data.

11. Refer to the waveform memories on sheet 3 of schematic -0644 and ensure $\overline{\text{SIN}}$ is low and each of the rest of the function select lines is high. A problem may be U6G, U2C, U11D or U12D. Program each function and check that appropriate memory is selected. Functions 15 through 21 will enable a group of memories in sequence if U13D, U14D and U11D circuits are functioning. Refer to table 6-6 as a troubleshooting aid.

12. Select function 2 (SQR) and check for eight address lines running at pins 4, 7, 9 and 12 of U11C and U12C. If not, ensure that pins 1 are low.

13. Check that each of eight data lines at pins 2, 5, 10 and 13 of U7F and U8F are a 195.31 Hz TTL square. Check pins 1, 4, 10 and 13 of U9F and U10F for the same signal. Sync to the sync output and check that these lines reverse phase when amplitude is programmed to a negative value.

14. Press RESET and check Q outputs of U10G for square wave signal. These should also appear at U12H data inputs.

5. Check TP10 for a 10V peak-to-peak square wave. If bad, ensure that the +5V reference at TP13 and ±15V analog supplies are ok before replacing U12H or U11H.

16. Program amplitude 10V and check TP11 for a 10V peak-to-peak square wave. If missing, check data inputs of U5H for a binary 1000 before changing U5H or U4H. Also ensure that U7G is receiving signals and producing clocks to associated data registers.

17. Ensure that offset is programmed to 0V and check TP12 for no offset. If bad, check U3H data inputs for a binary 512 before working on offset D/A circuit.

18. If signals are ok at TP11 and TP12, but bad at J26, troubleshoot output amplifier.

Table 6-5. Generator Troubleshooting

Symptom	Further Observations	Probable Cause
1. No output from ARB OUT (ATTEN) BNC.	1. Output at ARB OUT (HI), but not at ARB OUT (ATTEN).	1. Enable output. 2. U3G not sending ATTEN lines or not being clocked by U7G or pin 1 not high. 3. U2B. 4. K4, K5, K6, K7. 5. Coax from J27.
	2. No output at ARB OUT (HI).	Perform the functional test in this section.
2. No sync output.		$\overline{\text{END}}$ data, U8B, U10B, U10C, U11D, U8C.
3. No cursor output.	1. In partial block mode.	Address X not between start and stop address.
	2. In full block mode.	$\overline{\text{CUR}}$ data, U3B, U4B, U8C, U16D, U17D.
4. Partial block. Mode not working properly.	1. Works OK in full block and sync output OK.	1. PART data from U15A. 2. STRT data from U11A (high true binary). 3. $\overline{\text{END}}$ data from U10A (low true binary). 4. U9C, U10C, U13C.
	2. Doesn't work in full block or sync output not OK.	Perform functional test.
5. Trigger mode not working properly.	1. Generator does not stop in trigger mode.	1. TRIG line from U15A. 2. U16C and associated circuitry.
	2. Not triggering on, or in monitor mode, no holding.	Trigger logic circuitry and coax cables at J21 and J22.
	3. Some or all preset lengths do not function.	1. U6B and U7B. 2. $\overline{\text{LNTH}}$ low true BCD data. 3. U5B, U5C, U7C, U6C. 4. U7D, U15C.

Table 6-5. Generator Troubleshooting (Continued)

Symptom	Further Observations	Probable Cause
	4. Preset mode works, but MNTR CNT not displayed on front panel.	1. $\overline{\text{RBNK2}}$ and $\overline{\text{RBNK3}}$. 2. U6A and U8A.
6. Problem with REF IN or OUT.		1. $\overline{\text{INT}}$/EXT data from U15A. 2. U17B circuitry. 3. Coax cables to J19 or J20.
7. Problem with HOLD LED on front panel.		1. $\overline{\text{LED}}$. 2. $\overline{\text{RBNK1}}$. 3. U4C circuitry.
8. Ramp to zero from rear panel BNC bad.		1. $\overline{\text{RBNK1}}$. 2. U4C circuitry. 3. Coax cable to J23.
9. Inverted waveform (minus amplitude) bad.		1. INV data from U3G. 2. U7F, U8F, U9F, U10F.
10. ADRS X not displaying on front panel when HOLD key pressed.		1. $\overline{\text{RBNK0}}$. 2. U12A.
11. Not writing data to RAM.		1. Function B3 data. 2. $\overline{\text{ANAMEM}}$, WE ANALOG, and B$\overline{\text{R}}$/W signals. 3. U2F, U4E, U5E.
12. Not displaying Y data.		1. $\overline{\text{ANAMEM}}$, B$\overline{\text{R}}$/W. 2. U2F.
13. Smoothing problem.		1. Shorter than 20 μs sample time. 2. Check calibration.
	1. INTERP 1 through 64 lines at U15G and U16G not running.	U14F, U15F circuitry.
	2. All $\overline{Q}$ output of B register not running.	U11G, U12G.
	3. Program a SIN function. Square wave not present at U17E pin 4 at generator frequency.	U13G, U14G.
	4. |A−B| D/A data 4, 8, 16 not running or 32, 64, 128 high.	U13G, U14G, U17G, U18G.
	5. LC high.	U17F.
	6. INT D/A data 1 to 64 not running.	U15G, U16G.

Table 6-5. Generator Troubleshooting (Continued)

Symptom	Further Observations	Probable Cause
	7. No low level positive or negative ramps generated at TP4.	U17H, U15H, U14H.
	8. K1 and K2 not energized or K3 energized.	1. U16F, U18F. 2. SMOOTH data from U3G. 3. H1 RNG low.
	9. No +9V to −9V approximately 400 ns negative pulse at sample time at Q3 collector.	1. U8G. 2. Q2, A3 circuitry.
	10. Still no smoothing.	Q1, U8H circuitry.

Table 6-6. Function Decode

No.	Function	B4	B3	B2	B1	B0
0	SIN	L	L	L	L	L
1	TRI	L	L	L	L	H
2	SQR	L	L	L	H	L
3	RMP	L	L	L	H	H
4	PROM 1	L	L	H	L	L
5	PROM 2	L	L	H	L	H
6	PROM 3	L	L	H	H	L
7	PROM 4	L	L	H	H	H
8	RAM 1	L	H	L	L	L
9	RAM 2	L	H	L	L	H
10	RAM 3	L	H	L	H	L
11	RAM 4	L	H	L	H	H
15	PROM 1 + 2	H	L	H	L	H
16	PROM 1 + 2 + 3	H	L	H	H	L
17	PROM 1 + 2 + 3 + 4	H	L	H	H	H
19	RAM 1 + 2	H	H	L	L	H
20	RAM 1 + 2 + 3	H	H	L	H	L
21	RAM 1 + 2 + 3 + 4	H	H	L	H	H

SECTION 7
PARTS AND SCHEMATICS

7.1 DRAWINGS

The following assembly drawings (with parts lists) and schematics are in the arrangement shown below.

7.2 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, board, serial number of unit, and, if applicable, the function performed.

7.3 ERRATA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, errata pages are prepared to summarize the changes made and are inserted inside the shipping carton with this manual. If no such pages exist, the manual is correct as printed.

DRAWING	DRAWING NUMBER
Instrument Schematic	0004-00-0131
Chassis Assembly	0102-00-0666
Chassis Parts List	1101-00-0666
Front Panel Assembly	0102-00-0665
Front Panel Parts List	1101-00-0665
Display Board Schematic	0103-00-0640
Display Board Assembly	1100-00-0640
Display Board Parts List	1100-00-0640
Generator Board Schematic	0103-00-0644
Generator Board Assembly	1100-00-0644
Generator Board Parts List	1100-00-0644
Microprocessor/GPIB Board Schematic	0103-00-0660
Microprocessor/GPIB Board Assembly	1100-00-0660
Microprocessor/GPIB Board Parts List	1100-00-0660
Power Supply Schematic	0103-00-0659
Power Supply Assembly	1100-00-0659
Power Supply Assembly	0101-00-0659
Power Supply Parts List	1100-00-0659
Heat Sink Assembly	0102-00-0668
Heat Sink Parts List	1101-00-0668
Rear Panel Assembly	0102-00-0667
Rear Panel Parts List	1101-00-0667

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REV	ECN	BY	DATE	APP

REAR PANEL ASSEMBLY
(1101-00-0667)

POWER CORD: HOT BRN, GRN/YEL, WHT BLU

S2 CORCOM 6J1

F1

CR1 MDA990-1

F2

HEATSINK ASSEMBLY
(1101-00-0668)

Q18 7805 (IN, COM, OUT)

Q7 2N6486

Q14 2N6489

CR24 2N6504

C10 .01/50V

R1 .1Ω 10W

Q1 2N6489

Q2 TIP36

C1 5000 µf 15V

C2 .1/20V

C3 .1/20V

T1

CHASSIS

J14/P14 — J1/P1 — J16/P16

POWER SUPPLY BOARD
(1100-00-0659)

CHASSIS
0102-00-0666

J7 (TEST)

J8 (TEST)

J10 P10 (SIGNAL)

J4 P4 (POWER)

FLOATING GND.

J19 EXT REF IN
J20 REF OUT
J21 EXT HOLD
J22 EXT TRIG
J23 RAMP TO ZERO
J24 SYNC OUT
J25 CURSOR OUT
J26 ARB OUT (HI)
J27 ARB OUT (ATTEN)

V1

CHASSIS

J15/P15

GRN
RED
WHT
BLK
GRN/YEL

S1 POWER (ON / OFF)

J5 P5 (POWER)

MICROPROCESSOR/GPIB BOARD
(1100-00-0660)

ARBITRARY GENERATOR BD.
(1100-00-0644)

J18 P18 WORD GENERATOR (OPTION)

J17 GPIB (GPIB)

FRONT PANEL ASSEMBLY
(1101-00-0665)

J6/P6 (POWER)

J11/P11 (SIGNAL)

DISPLAY BOARD
(1100-00-0640)

P28 J28 KEYBOARD
(5108-00-0003)

NOTE. UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 3-8-78	WAVETEK SAN DIEGO • CALIF
MATERIAL	PROJENGR		TITLE: SCHEMATIC INSTRUMENT
FINISH WAVETEK PROCESS	RELEASE APPROV 6-9-78		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.030 ANGLES ±1°		
	DO NOT SCALE DWG		MODEL NO 175 / DWG NO 0004-00-0131 / REV A
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

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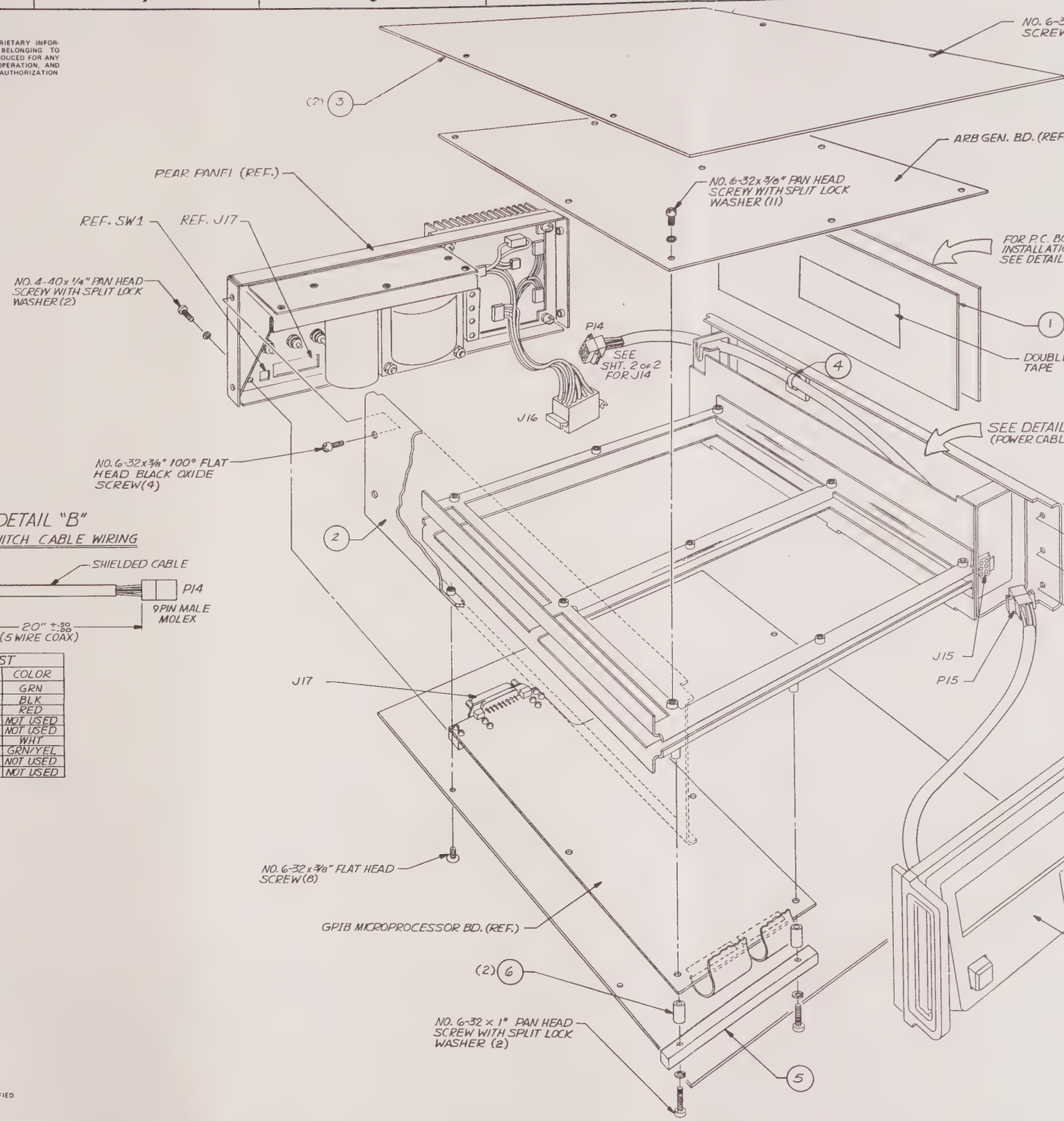
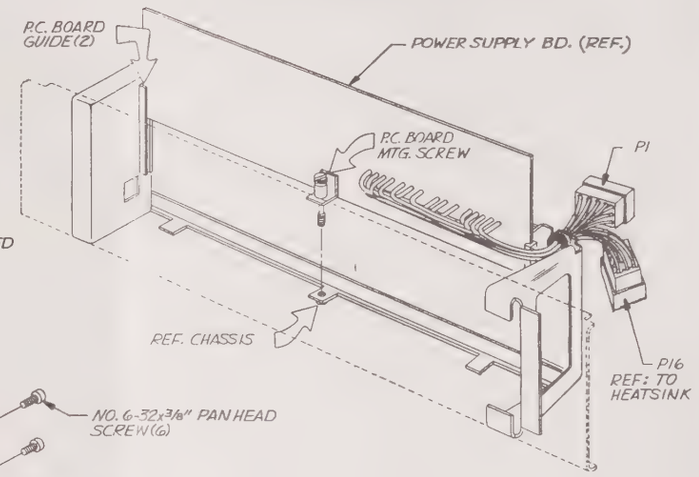
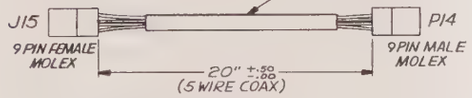
REV	ECN	BY	DATE	APP
B	ECN 2070	[illegible]	1-6-80	
	3A: F (CL III)	[illegible]	7/16	[illegible]
C	7128	[illegible]	2-28-83	[illegible]


NO. 6-32x3/8" 100° FLAT HEAD BLACK OXIDE SCREW (8) (REF.)
(2) 3
ARB GEN. BD. (REF.)
REAR PANEL (REF.)
NO. 6-32x3/8" PAN HEAD SCREW WITH SPLIT LOCK WASHER (11)
REF. SW1
REF. J17
NO. 4-40x1/4" PAN HEAD SCREW WITH SPLIT LOCK WASHER (2)
P14
SEE SHT. 2 OF 2 FOR J14
J16
FOR P.C. BOARD INSTALLATION SEE DETAIL "A"
1
DOUBLE SIDED TAPE
4
SEE DETAIL "B" (POWER CABLE)
NO. 6-32x3/8" 100° FLAT HEAD BLACK OXIDE SCREW(4)
2
NO. 6-32x3/8" PAN HEAD SCREW(6)
J15
P15
J17
NO. 6-32x3/8" FLAT HEAD SCREW(8)
GPIB MICROPROCESSOR BD. (REF.)
(2) 6
NO. 6-32x1" PAN HEAD SCREW WITH SPLIT LOCK WASHER (2)
5
FRONT PANEL (REF.)

DETAIL "A"
P.C. BOARD INSTALLATION



DETAIL "B"
POWER SWITCH CABLE WIRING



WIRE LIST		
PIN NO	WIRE GA.	COLOR
1	20	GRN
2	20	BLK
3	20	RED
4		NOT USED
5		NOT USED
6	20	WHT
7	20	GRN/YEL
8		NOT USED
9		NOT USED

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 3-17-83
MATERIAL	PROJ ENGR	
	RELEASE APPROV [signature] 4-9-83	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030	
	DO NOT SCALE DWG	
	SCALE	

WAVETEK SAN DIEGO • CALIFORNIA

TITLE: ASSEMBLY CHASSIS

MODEL NO	DWG NO	REV
175	0102-00-0666	C
CODE IDENT 23338	SHEET 1 OF 2	

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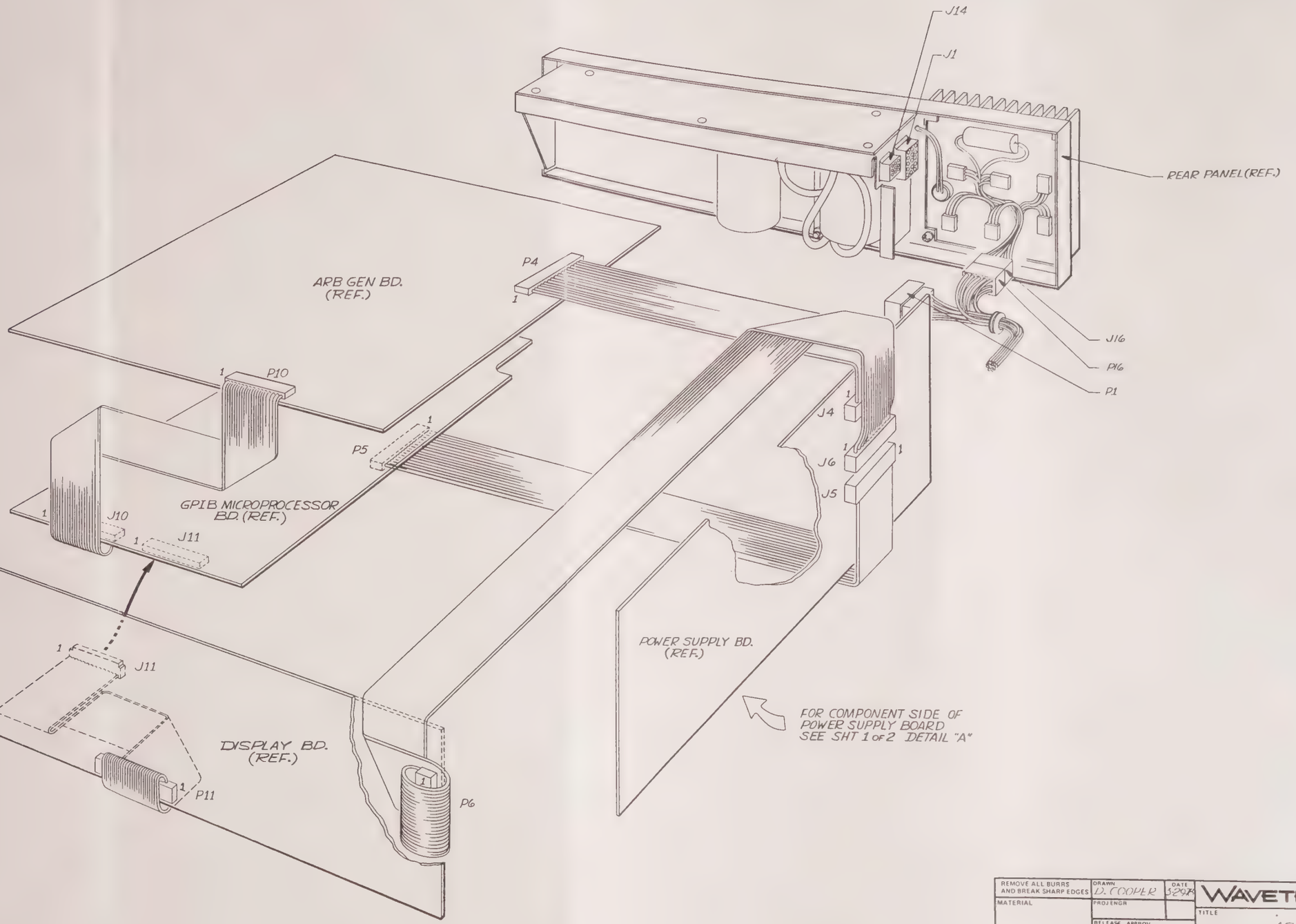
REV	ECN	BY	DATE	APP



NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 9-29-78	WAVETEK SAN DIEGO, CALIF.
MATERIAL	PROJ ENGR		TITLE ASSEMBLY CHASSIS
FINISH WAVETEK PROCESS	RELEASE APPROV S. Cook 9-78		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 175
	SCALE		DWG NO 0108-00-0666 REV C
			CODE IDENT 23338 SHEET 2 OF 2

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, CHASSIS	0102-00-0666	WVTK	0102-00-0666	1
NONE	ASSY, 4 CONDUCTOR CABLE 175-0666	175-2084	WVTK	1207-00-2084	1
NONE	MTG BKT	172-6332	WVTK	1400-00-6332	2
1	SHIELD, PWR SUPPLY REF 3200-03-0004	175-8480	WVTK	1400-00-8480	1
2	CHASSIS	30501	CALMK	1400-00-8670	1
3	COVER	30501-2	CALMK	1400-00-8680	2
5	SUPPORT BAR	175-5673	WVTK	1400-01-5673	1
J15	CONN, 9PIN	03-06-1091	MOLEX	2100-02-0010	1
P14	PLUG, 9PIN	03-06-2091	MOLEX	2100-02-0011	1
NONE	PIN, FEMALE	350628-1	AMP	2100-05-0002	5
NONE	PIN, MALE	350629-1	AMP	2100-05-0003	5
NONE	CARD GUIDES	120-400	CALMK	2100-06-0017	2
4	MOUNT, ADHESIVE	ABMS-A-C	PANDT	2800-00-0001	1
6	SPACER .562 H, .250 DIA 140 DIA THRU	8713	SMITH	2800-04-0004	2
2	PRESS NUT, 10-32	SS-032-2	PEM	2800-16-0021	8

WAVETEK PARTS LIST	TITLE: CHASSIS	ASSEMBLY NO. 1101-00-0666	REV E

PAGE 1

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST CHASSIS
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.030 ANGLES ±1		
	DO NOT SCALE DWG	MODEL NO 175	DWG NO 1101-00-0666 REV E
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3694

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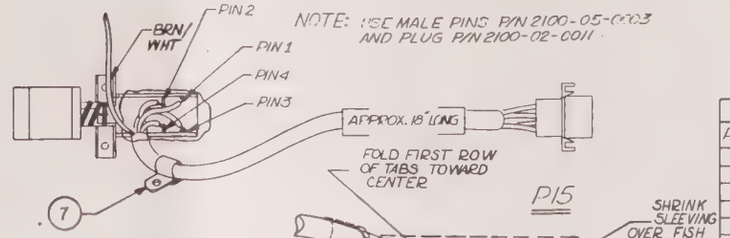
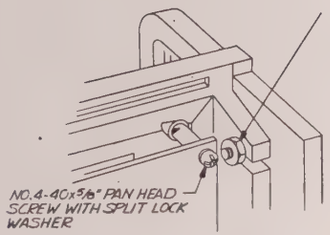
REV	ECN	BY	DATE	APP



NOTE: USE MALE PINS P/N 2100-05-0003 AND PLUG P/N 2100-02-0011

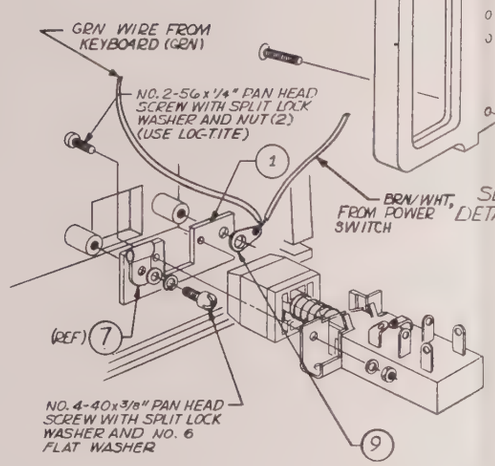
P15 WIRE LIST

PIN NO.	WIRE GA.	COLOR	DESTINATION
1	20	GRN	S1-2
2	20	BLK	S1-3
3	20	RED	S1-1
4		NOT USED	
5		NOT USED	
6	20	WHT	S1-4
7	20	WHT/BRN	SHIELD
8		NOT USED	
9		NOT USED	

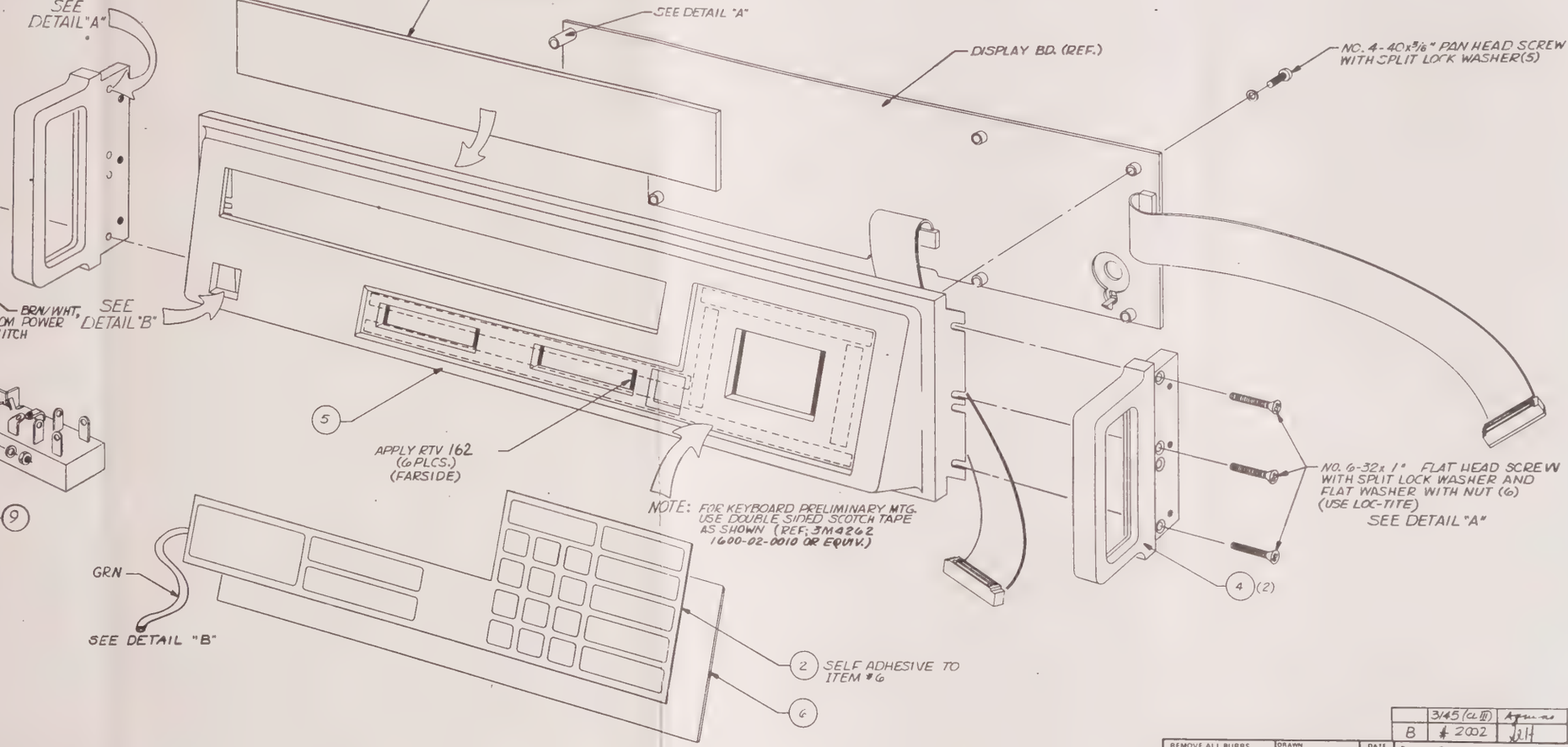


CAUTION MUST BE TAKEN IN THIS AREA DUE TO POSSIBLE INTERFERENCE WITH P.C. BOARD, SCREW NOT TO HAVE LOCK WASHER USE LOC-TITE ONLY

DETAIL "A"


GRN WIRE FROM KEYBOARD (GRN)
NO. 2-56 x 1/4" PAN HEAD SCREW WITH SPLIT LOCK WASHER AND NUT (2) (USE LOC-TITE)
1
BRN/WHT FROM POWER SWITCH
(REF) 7
NO. 4-40 x 3/8" PAN HEAD SCREW WITH SPLIT LOCK WASHER AND NO. 6 FLAT WASHER
9

DETAIL "B"
S1 HARDWARE STACK-UP


SEE DETAIL "A"
SEE DETAIL "B"
3 INSTALL BY USING HOT GLUE ALL 4 SIDES
SEE DETAIL "A"
DISPLAY BD. (REF.)
NO. 4-40 x 3/16" PAN HEAD SCREW WITH SPLIT LOCK WASHER(S)
5
APPLY RTV 162 (6 PLCS.) (FARSIDE)
NO. 6-32 x 1" FLAT HEAD SCREW WITH SPLIT LOCK WASHER AND FLAT WASHER WITH NUT (6) (USE LOC-TITE)
SEE DETAIL "A"
4 (2)
NOTE: FOR KEYBOARD PRELIMINARY MTG. USE DOUBLE SIDED SCOTCH TAPE AS SHOWN (REF: 3M4262 1600-02-0010 OR EQUIV.)
GRN
SEE DETAIL "B"
2 SELF ADHESIVE TO ITEM #6
6

NOTE: UNLESS OTHERWISE SPECIFIED

	3145 (ECN III)		6/2/82	
B	# 2002	JH	7-19-79	

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 3-14-79	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE ASSEMBLY FRONT PANEL
FINISH WAVETEK PROCESS	RELEASE APPROV 6-9-75		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 175
	SCALE		DWG NO 0102-00-0665 REV B
			CODE IDENT 23338 SHEET 1 OF 1

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, FR PANEL	0102-00-0665	WVTK	0102-00-0665	1
NONE	ASSY, 4 CONDUCTOR CABLE 175-0665	175-2083	WVTK	1207-00-2083	1
1	BRKT, SWITCH MTG.	172-7703	WVTK	1400-00-7703	1
2	OVERLAY, KEYBOARD	175-8160	WVTK	1400-00-8160	1
3	PANEL, PLEX DISPLAY	175-8230	WVTK	1400-00-8230	1
NONE	INSULATOR, PWR SWITCH REF 1600-99-0001	801-8370	WVTK	1400-00-8370	2
5	FRONT PANEL, MODIFIED FROM 1400-00-7031	175-8469	WVTK	1400-00-8469	1
4	HANDLE, WHITE FROM 1400-00-6951	172-3152	WVTK	1400-01-3152	2
P15	PLUG, 9PIN	03-06-2091	MOLEX	2100-02-0011	1
9	SOLDER LUG	11A144	ZIER	2100-04-0025	1
NONE	PIN, MALE	350629-1	AMP	2100-05-0003	5
NONE	TIE MOUNT	TM-256C	PANDT	2800-00-0005	1
7	CABLE CLAMP	770-1505	CONCD	2800-00-0010	1
S1	SWITCH, POWER	5102-00-0006	WVTK	3102-00-0006	1
6	KEYBOARD	2SMD200P75079	CRL	3108-00-0003	1

WAVETEK PARTS LIST	TITLE: FRONT PANEL	ASSEMBLY NO.: 1101-00-0665	REV: B
		PAGE 1	

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST FRONT PANEL
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		MODEL NO: 175 / DWG NO: 1101-00-0665 / REV: B
	DO NOT SCALE DWG		CODE IDENT: 23338 / SHEET 1 OF 1
	SCALE		

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A3994

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REV	ECN	BY	DATE	APP
B	[illegible]	[illegible]	[illegible]	[illegible]
C	ECN 0121	DJC	4/15/80	

+15V
C4 22/15V TANT
Q1 2N3638
Q2 2N3642
CR12 FD666
R6 100
TONE TRANSDUCER MOLEX 15-24-2034 GULTN 101

74LS138 +5V U32
P11-34 WBNK5
P11-33 WE DISPLAY
P11-29 AD2
P11-16 AD1
P11-14 AD0

U22 74LS 273 +5V
P11-18 D7
P11-21 D6
P11-20 D5
P11-25 D4
P11-26 D3
P11-22 D2
P11-19 D1
P11-15 D0
SPARE
LMPTST (1A8)
CR1 CR2 CR3 CR4 CR5 CR6 CR7 CR8 CR9 CR10
R7 470 R8 470 R3 470 R9 470
U20 7404

U23 74LS 273 +5V
D7 D6 D5 D4 D3 D2 D1 D0
UAD3 UAD2 UAD1 LAD5 LAD4 LAD3 LAD2 LAD1

U24 74LS 273 +5V
DP4 DP3 DP2 DP1
CR13 CR14 CR15 CR16
R7 470 R8 470 R9 470

U25 74LS 273 +5V
RAM3 RAM2 RAM1
CR25 CR17 CR18 CR19 CR20
R8 470 R7 470

U21 74LS 175 +5V
CR21 CR22 CR23 CR24
R3 470 R2 470

+5V R8 470
CR26 CR27 CR28
RAM3 RAM2 RAM1

LED	FUNCTION
CR1	OUTPUT ON
CR2	SMOOTH ON
CR3	INT } CLK
CR4	EXT } CLK
CR5	PRST } COUNT
CR6	MNTR } COUNT
CR7	FULL } BLOCK
CR8	PART } BLOCK
CR9	CONT } MODE
CR10	TRIG } MODE
CR11	HOLD
CR13	RAMP
CR14	SQR
CR15	TRI
CR16	SIN
CR17	PROM 4
CR18	PROM 3
CR19	PROM 2
CR20	PROM 1
CR21	SRQ } GPIB
CR22	REM } GPIB
CR23	TLK } GPIB
CR24	LSN } GPIB
CR25	RAM 4
CR26	RAM 3
CR27	RAM 2
CR28	RAM 1

R10 6.81K Q3 R13 6.81K Q4 R16 6.81K Q5 R19 6.81K Q6 R22 6.81K Q7 R25 6.81K Q8 R28 6.81K Q9 R31 6.81K Q10 R34 6.81K Q11 R37 6.81K Q12 R40 6.81K Q13 R42 15
2N3638A (11 PLCS.)
R55 4.5K
R11 332 R12 15 PIN10 (U2-8)
R14 332 R15 15 PIN9 (U2-8)
R17 332 R18 15 PIN8 (U2-8)
R20 332 R21 15 PIN5 (U2-8)
R23 332 R24 15 PIN4 (U2-8)
R26 332 R27 15 PIN2 (U2-8)
R29 332 R30 15 PIN3 (U2-8)
R32 332 R33 15 DP4(IC5)
R35 332 R36 15 DP3(IC5)
R38 332 R39 15 DP2(IC5)
R41 332 R15 DP1(IC5)

74LS157 U31 +5V
74S189 U17 +5V
74S188(PROG) U16 +5V N.C.
P11-17 WBNK4
470 R3 +5V
U19 74LS 161
(2D8) CLK
C3 22/15V TANT +5V
R1 4.99K
R2 4.99K
C1 0.1uf 10% MYLAR
U30 555
C2 .01
C14 470 PF
74LS42 U18 +5V
SPARE N.C. N.C.
P11-30 BHOLD
LMPTST (IC7)
U15 74LS00
SIP R3 470 CR11 +5V
U20 7404

U2 DIGIT 1 Q14 2N3638A (7 PLCS)
U3 DIGIT 2 Q15
U4 DIGIT 3 Q16
U5 DIGIT 4 Q17
U6 DIGIT 5 Q18
U7 DIGIT 6 Q19
U8 DIGIT 7 Q20
3|2|4|5|8|9|10
1,6 7

TYPICAL (DIGIT 1 THRU 7)
HP5082-7740 (TIL313)

3. CAPACITANCE IN uF
2. RESISTORS ARE 1/4W 1% MF
1. LEDS ARE TIL-209A
NOTE UNLESS OTHERWISE SPECIFIED

LAST REF. DES. USED:
CR28 U32
Q37
R62
C14
P28

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D.COOPER	DATE 1-31-78	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE SCHEMATIC DISPLAY BOARD
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 115
	SCALE		DWG NO 010-00-0640 REV C
			CODE IDENT 23338 SHEET 1 OF 2

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REV	ECN	BY	DATE	APP

74LS245 +5V

C5 .01 +5V

U11

U10 74LS290

CLK (1B8)

U14 7414

Q21 2N3638A (10)

R43 499

Q22 R44 499

Q23 R45 499

Q24 R46 499

Q25 R47 499

Q26 R48 499

Q27 R49 499

Q28 R50 499

Q29 R51 499

Q30 R52 499

+5V

C8 22/15V TANT

U1 LABEL TIL305 (MAN2A)

U9 UNIT TIL305 (MAN2A)

R53 61.9 R57 61.9 R58 61.9 R59 61.9 R60 61.9 R61 61.9 R62 61.9

Q31 2N3638A(7) Q32 Q33 Q34 Q35 Q36 Q37

R54 10K SIP (7) +5V

R55 1.5K SIP (8) +5V

R56 10K SIP +5V

U14 7414 U15 74LS00 LAD5

U14 7414

R8 470 +5V

74LS157 +15V

(IC5) UAD3 UAD2 UAD1 LAD4 LAD3 LAD2 LAD1

U12

PROG. 74S471 C6 +5V .01

U13

C7 .01 +5V N.C. N.C.

74LS148 +5V U29

74LS138 U26

74LS293 U26

P11-15 D0 P11-19 D1 P11-22 D2 P11-18 D7 P11-3 RBNK4 P11-26 D3 P11-25 D4 P11-20 D5

U27 74LS 244 +5V

111 110 101 100 011 010 001 000

P28 J28

DISPLAY BD. KEY BD.(REF.)

KEY BOARD (FRONT VIEW)

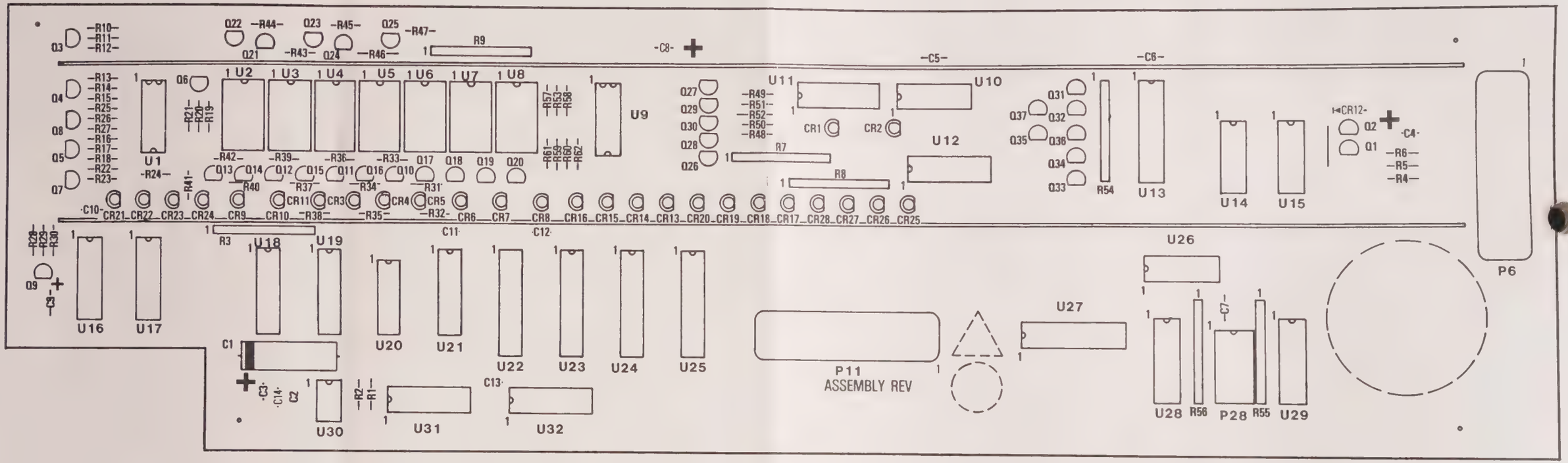
P/O POWER	P11 SIGNAL
→ 1	BM/IO → 1*
→ 2	BR/W → 2*
→ 3	RBNK4 → 3
+5V → 4	AD3 → 4*
→ 5	AD4 → 5*
→ 6	AD5 → 6*
→ 7	AD6 → 7*
→ 8	AD7 → 8*
→ 9	RESET → 9*
→ 10	BUFEN → 10*
→ 11	RBNK7 → 11*
+5V COM → 12	RBNK5 → 12*
→ 13	BOPREQ → 13*
→ 14	AD0 → 14
→ 15	D0 → 15
→ 16	AD1 → 16
→ 17	WBNK4 → 17
→ 18	D7 → 18
-15V → 19*	D1 → 19
+5V COM → 20	D5 → 20
±15V COM → 21*	D6 → 21
→ 22*	D2 → 22
→ 23	AD13 → 23*
+5V COM → 24	AD14 → 24*
→ 25	D4 → 25
+15V → 26	D3 → 26
→ 27	COM → 27
+5V COM → 28	WBNK6 → 28*
+5V ISO → 29*	AD2 → 29
→ 30*	BHOLD → 30
+5V COM → 31	WBNK7 → 31*
→ 32	COM → 32
→ 33*	WE DISPLAY → 33
ISO COM → 34*	WBNK5 → 34

* NOT USED

+5V C9 22/15V TANT C10 .01 C11 .01 C12 .01 C13 .01

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D COOPER	DATE 1-31-78	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC DISPLAY BOARD
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 175	DWG NO 0103-00-0640 REV C
	SCALE	CODE IDENT 23338	SHEET 2 OF 2



MADE FROM 0100-00-0640-3D

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK
MATERIAL	PROTENGR		TITLE: ASSEMBLY DISPLAY
	RELEASE APPROV		
FINISH: WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX .010 ANGLES 1°, XX .010		
	DO NOT SCALE DWG	MODEL NO: 175	DWG NO: 1100-00-0640
	SCALE	CODE IDENT: 23338	SHEET 1 OF 1

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, DISPLAY BD	0101-00-0640	WVTK	0101-00-0640	1
NONE	SCHEMATIC, DISPLAY BD	0103-00-0640	WVTK	0103-00-0640	1
C10 C11 C12 C13 C2 C5 C6 C7	CAP, CER, MN, .01MF, 50V	QE50-103ZA	MURAT	1500-01-0310	8
NONE	CAP, CER, 470PF, 1KV	DD-471	CRL	1500-04-7111	1
C1	CAP, MYLR, .1MF, 100V	WMF1P1	CDE	1500-41-0424	1
C3 C4 C8 C9	CAP, TANT, 22MF, 15V	196D226X9015KA1	SPRAG	1500-72-2601	4
NONE	DISPLAY BOARD	175-0640	WVTK	1700-00-0640	1
NONE	SPACER, SWAGE .125 H, .250 DIA	B1570-B-1/8-11	USECO	2800-04-0008	5
NONE	SPACER, SWAGE .375 H, .250 DIA	B1570-B-3/8-11	USECO	2800-04-0009	1
7	SCREW, PAN, SLOTED, TYPE B, 2 X 1/4	2 X 1/4 PAN	CMRCL	2800-22-2104	2
NONE	SPACER, L.E.D.	906-310	BIVAR	3000-00-0036	27
NONE	BEEPER	KBS-27DB-3A	KYCRA	3000-00-0068	1
R6	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	1
R4	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	1
R12 R15 R18 R21 R24 R27 R30 R33 R36 R39 R42	RES, MF, 1/8W, 1%, 15	RN55D-15R0F	TRW	4701-03-1509	11

WAVETEK PARTS LIST | TITLE: PCA, DISPLAY BD | ASSEMBLY NO. 1100-00-0640 | REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R5	RES, MF, 1/8W, 1%, 3.01K	RN55D-3011F	TRW	4701-03-3011	1
R11 R14 R17 R20 R23 R26 R29 R32 R35 R38 R41	RES, MF, 1/8W, 1%, 332	RN55D-3320F	TRW	4701-03-3320	11
R43 R44 R45 R46 R47 R48 R49 R50 R51 R52	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	10
R1 R2	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	2
R53 R57 R58 R59 R60 R61 R62	RES, MF, 1/8W, 1%, 61.9	RN55D-61R9F	TRW	4701-03-6199	7
R10 R13 R16 R19 R22 R25 R28 R31 R34 R37 R40	RES, MF, 1/8W, 1%, 6.81K	RN55D-6811F	TRW	4701-03-6811	11
R54 R56	RES MODULE, 10K	4310R-101-103	BOURN	4770-00-0008	2
R3 R7 R8 R9	RES MODULE	4310R-101-471	BOURN	4770-00-0009	4
R55	RES NETWK	785-1R1.5K	BECK	4770-00-0010	1
CR12	DIODE	1N4148	FAIR	4807-02-6666	1
U2 U3 U4 U5 U6 U7 U8	LED	HDSP-3106	HP	4899-00-0009	7
U1 U9	LED	TIL-305	TI	4899-00-0013	2
CR1 CR10 CR11 CR13 CR14 CR15 CR16 CR17 CR18 CR19 CR2 CR20 CR21 CR22 CR23 CR24 CR25 CR26 CR27 CR28 CR3 CR4 CR5 CR6 CR7 CR8 CR9	LED	MV5774B	MONSO	4899-00-0014	27

WAVETEK PARTS LIST | TITLE: PCA, DISPLAY BD | ASSEMBLY NO. 1100-00-0640 | REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
Q10 Q11 Q12 Q13 Q14 Q15 Q16 Q17 Q18 Q19 Q20 Q21 Q22 Q23 Q24 Q25 Q26 Q27 Q28 Q29 Q3 Q30 Q31 Q32 Q33 Q34 Q35 Q36 Q37 Q4 Q5 Q6 Q7 Q8 Q9	TRANS	2N3638A	CARTR	4901-03-6381	35
Q1 Q2	TRANS	2N3642	FAIR	4901-03-6420	2
P28	CABLE ASSY	CA-D141DSP-E-CD-005	CA	6002-00-0003	1
P11	ASSY, RIBBON CABLE	922522-34-02-11	AP	6002-00-0006	1
P6	ASSY, RIBBON CABLE	922522-34-02-22	AP	6002-00-0007	1
NONE	POWER BUSS BAR (ST)	6009-90-0005	WVTK	6009-90-0005	2
U30	IC	NE555V	SIG	7000-05-5500	1
U15	IC	74LS00	TI	8000-74-0010	1
U20	IC	7404	TI	8000-74-0400	1
U14	IC	7414	TI	8000-74-1400	1
U11 U18	IC	74LS42B	SIG	8000-74-4210	2
U28 U32	IC	74LS138	TI	8007-41-3810	2
U29	IC	74LS148	TI	8007-41-4810	1
U12 U31	IC	74LS157	TI	8007-41-5710	2

WAVETEK PARTS LIST | TITLE: PCA, DISPLAY BD | ASSEMBLY NO. 1100-00-0640 | REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U19	IC	74LS161	SIG	8007-41-6110	1
U21	IC	74LS175	TI	8007-41-7510	1
U17	IC	N74S189A	SIG	8007-41-8900	1
U27	IC	74LS244	TI	8007-42-4410	1
U22 U23 U24 U25	IC	74LS273	TI	8007-42-7310	4
U10	IC	74LS290	TI	8007-42-9010	1
U26	IC	74LS293	TI	8007-42-9310	1
U13	IC, PROGRAMMED REF 8007-44-7101	8600-00-0128	WVTK	8600-00-0128	1
U16	IC, PROGRAMMED REF 8007-41-8801	8600-00-0129	WVTK	8600-00-0129	1

WAVETEK PARTS LIST | TITLE: PCA, DISPLAY BD | ASSEMBLY NO. 1100-00-0640 | REV D

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PCA, DISPLAY BD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 175 | DWG NO 1100-00-0640 | REV D
	SCALE		CODE IDENT 23338 | SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

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REV	ECN	BY	DATE	APP

DATA REGISTERS

+5V — C60 THRU C72 22 µf/15V TANT

(PIO-34) WBNK1
(PIO-33) WE ANALOG
(PIO-1) AD2
(PIO-2) AD1
(PIO-6) AD0
U7G 74LS 138 → RESTART (2C8), µPSTART (1A6), µPHOLD (1A7)

WBNK0 (PIO-30)
U16A 74LS 138

R1 10K, C1 TANT 22/15V

U3G 74LS 273: AMPL 2, AMPL 1, INV, SMOOTH, ATTEN 1, ATTEN .1, ATTEN .01, ATTEN .001

U4G 74LS 273: +/- OFST, OFST 256, OFST 128, OFST 64, OFST 32, OFST 16, OFST 8, OFST 4

U6G 74LS 273: OFST 2, OFST 1, SPARE, FUNC B4, FUNC B3, FUNC B2, FUNC B1, FUNC B0

U5G 74LS 273: AMPL 512, AMPL 256, AMPL 128, AMPL 64, AMPL 32, AMPL 16, AMPL 8, AMPL 4

(1C5) FUNC B3, FUNC B2 — (2B3) FUNC C1, FUNC C0 → (2C1), (2B1)

R3 2.21K

U2C 74LS 138: PROM 4 (2B3), PROM 3 (2B3), PROM 2 (2B4), PROM 1 (2B5), RAMP (2B7), SQR (2B8), TRI (2C6), SIN (2B5)

(PIO-31) D7
(PIO-28) D6
(PIO-26) D5
(PIO-24) D4
(PIO-25) D3
(PIO-27) D2
(PIO-29) D1
(PIO-32) D0
U15A 74LS 273 (TYP 12): INT/EXT, PRST, PART, TRIG, RD4, RD2, RD1, SPARE

TO D-INPUTS OF ALL REGISTERS

R2 1K

U13A 74LS 273: STD 8000, STD 4000, STD 2000, STD 1000, STD 800, STD 400, STD 200, STD 100

U14A 74LS 273: STD 80, STD 40, STD 20, STD 10, STD 8, STD 4, STD 2, STD 1

U11A 74LS 273: STRT 128, STRT 64, STRT 32, STRT 16, STRT 8, STRT 4, STRT 2, STRT 1

U10A 74LS 273: END 128, END 64, END 32, END 16, END 8, END 4, END 2, END 1

U7A 74LS 273: LNTH 8000, LNTH 4000, LNTH 2000, LNTH 1000, LNTH 800, LNTH 400, LNTH 200, LNTH 100

U5A 74LS 273: LNTH 80, LNTH 40, LNTH 20, LNTH 10, LNTH 8, LNTH 4, LNTH 2, LNTH 1

U4A 74LS 273: CUR 128, CUR 64, CUR 32, CUR 16, CUR 8, CUR 4, CUR 2, CUR 1

POWER SUPPLY J4

+5V: 1, 2, 3, 4, 5, 6
+5V COM: 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18
-15V: 19
+15V COM: 20
±15V COM: 21, 22, 23
+5V COM: 24, 25
+15V: 26
+5V COM: 27, 28
+5V ISO: 29*, 30*
+5V COM: 31, 32
+5V ISO COM: 33*, 34*

*= NOT USED

µP/GPIB PIO

AD2 → 1, AD1 → 2, AD4 → 3, AD5 → 4, AD3 → 5, AD0 → 6, AD7 → 7, AD4 → 9, * AD8 → 9, * AD9 → 10, * AD10 → 11, COM → 12, 10MHz → 13, COM → 14, RBNK1 → 15, BHOLD → 16, * WBNK3 → 17, BR/W → 18, ANAMEM → 19, RBNK3 → 20, RBNK2 → 21, * WBNK2 → 22, RBNK0 → 23, D4 → 24, D3 → 25, D5 → 26, D2 → 27, D6 → 28, D1 → 29, WBNK0 → 30, D7 → 31, D0 → 32, WE ANALOG → 33, WBNK1 → 34

TP14 TP15 TP16 TP17 TP18 TP19 TP20

+5V COM — ±15V COM — A

SAMPLE TIME GENERATOR

STD1 STD2 STD4 STD8 (1C5) STD10 STD20 STD40 STD80 (1C6) STD100 STD200 STD400 STD800 STD1000 STD2000 STD4000 STD8000

U15B 74LS192 — U16B 74LS192 — U13B 74LS192 — U14B 74LS192

R7 2.21K

TP1 TP2 TP3

(PIO-13) 10 MHz

INT/EXT (1C7)
EXT REF IN (J-19)
CR1 R4 2.21K CR2
74132 U17B

REF OUT (J-20)
U16D 7404 U16D

U13C 7402 — U15C 7410 — U13C 7402

U14C 7474: D, SD, CLK, CD, Q, Q̄ — PUP (2C7) — CLK (2C7)

R8 2.21K

U16F 7404 — BHOLD (PIO-16)

U16E 7400 — U16E 7400 — U16E 7400 — U16G 7410

TP5 — U16F 7404 — RNG CLK (2D8)

TRIGGER LOGIC

R5 2.21K, CR3
EXT HOLD (J-21), CR4, R6 2.21K
EXT TRIG (J-22), CR5

U14C 74132 — µPHOLD (1D7) — U10C 7404

U10C 7404 — U4C 74132 — C2 .0022 mf DISC

TRIG (1C7) — U15C 7410 — µPSTART (1D7)

U10C 7404 — TP4 — UNTH CLR (2B7) (2D1) — UNTH CLR (2A4)

(2A3) STOP — U16C 7410 — HOLD (2B4)

U16C 7410 — HOLD (2D5) (2D6)

1. RESISTORS ARE ¼W, 1%, M.F.
2. DIODES ARE FD6666

NOTE UNLESS OTHERWISE SPECIFIED

G	4824	SC	10 18 85
F	ECN 2815	FNA	4/12
E	ECN 2122	MJE	4/19/82
D	ECN 1798	RO	8/24/78

REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN D. COOPER | DATE 2-17-78
MATERIAL | PROJ ENGR | RELEASE APPROV 6-9-78
FINISH WAVETEK PROCESS | TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030
DO NOT SCALE DWG | SCALE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: SCHEMATIC ARB GEN

MODEL NO 175 | DWG NO 0103-00-0644 | REV G
CODE IDENT 23338 | SHEET 1 OF 4

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REV	ECN	BY	DATE	APP

RANGE SELECTOR

INTERPOLATION COUNTER

ADDRESS COUNTER

LENGTH COUNTER

SYNC OUTPUT

CURSOR OUTPUT

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D.COOPER	DATE 2-1-78	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE SCHEMATIC A2B GEN
FINISH WAVETEK PROCESS	RELEASE APPROV 6-4-78		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO 175	DWG NO 0103-00-0644 REV G
	SCALE	CODE IDENT 23338	SHEET 2 OF 4

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REV	ECN	BY	DATE	APP

WORD GENERATOR OPTION

WAVEFORM MEMORY

U9F 74LS283 · U10F 74LS283 · U8F 74LS86 · U7F 74LS86 · U5D 74LS244 · U4D 74LS273 · U6D 7404 · U11F 74LS244 · U11E 74LS244 · U12E 74LS244 · U12F 74LS86 · U13F 74LS86 · U6E 74S471 TYP. (5) · U7E 74S471 OPT. · U8E 74S471 OPT · U9E 74S471 OPT · U10E 74S471 OPT · U11C 74LS157 · U12C 74LS157 · U13E · U14E 74LS05 · U14E 74LS05 · U3C 74LS132 · U2F 74LS245 · U4E 2114 · U5F 2114 · R22 2.21K · R23 2.21K · R24 2.21K · R25 1K · R26 1K · R27 1K · R28 1K · R29 1K

74LS05 (10PLCS.)

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 2/78	WAVETEK SAN DIEGO, CALIF.
MATERIAL	PROJ ENGR		TITLE SCHEMATIC ARB GEN.
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 175	DWG NO 0103-00-0644 REV G
	SCALE	CODE IDENT 23338	SHEET 3 OF 4

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REV	ECN	BY	DATE	APP

A REGISTER

B REGISTER

INTERPOLATOR D/A

FUNCTION D/A

AMPLITUDE D/A

SAMPLE/HOLD

OFFSET D/A

ATTENUATOR

OUTPUT AMPLIFIER

MATCHED SET 5
4.99K RESISTORS
WVTK*4789-00-0044

SOURCE SUB DRAIN

GATE

SOURCE IMPEDANCE JUMPER

AMPL OUT (4A5)

OFST OUT (4A5)

VREF (4B1)

INT D/A 128 (4D4)

AMPL OUT (4D1)

OFST OUT (4C1)

S/H OFF (4C5)

J-26 ARB OUT (HI)

J-27 ARB OUT (ATTEN)

ATTEN 1 (1C6)

ATTEN .1 (1C6)

ATTEN .01 (1C6)

ATTEN .001 (1C6)

HEAT SINK

2. CAPACITANCE IN uf, CERAMIC DISC.
1. A ⏚ = ANALOG COM

NOTE: UNLESS OTHERWISE SPECIFIED

LAST REF. DES. USED:

CR18	Q9
TP20	K7
R107	C72

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 2-78	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC ARB GEN.
FINISH WAVETEK PROCESS	RELEASE APPROV 6-4-78		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG		MODEL NO 175
	SCALE		DWG NO. 0103-00-0644 REV G
			CODE IDENT 23338 SHEET 4 OF 4

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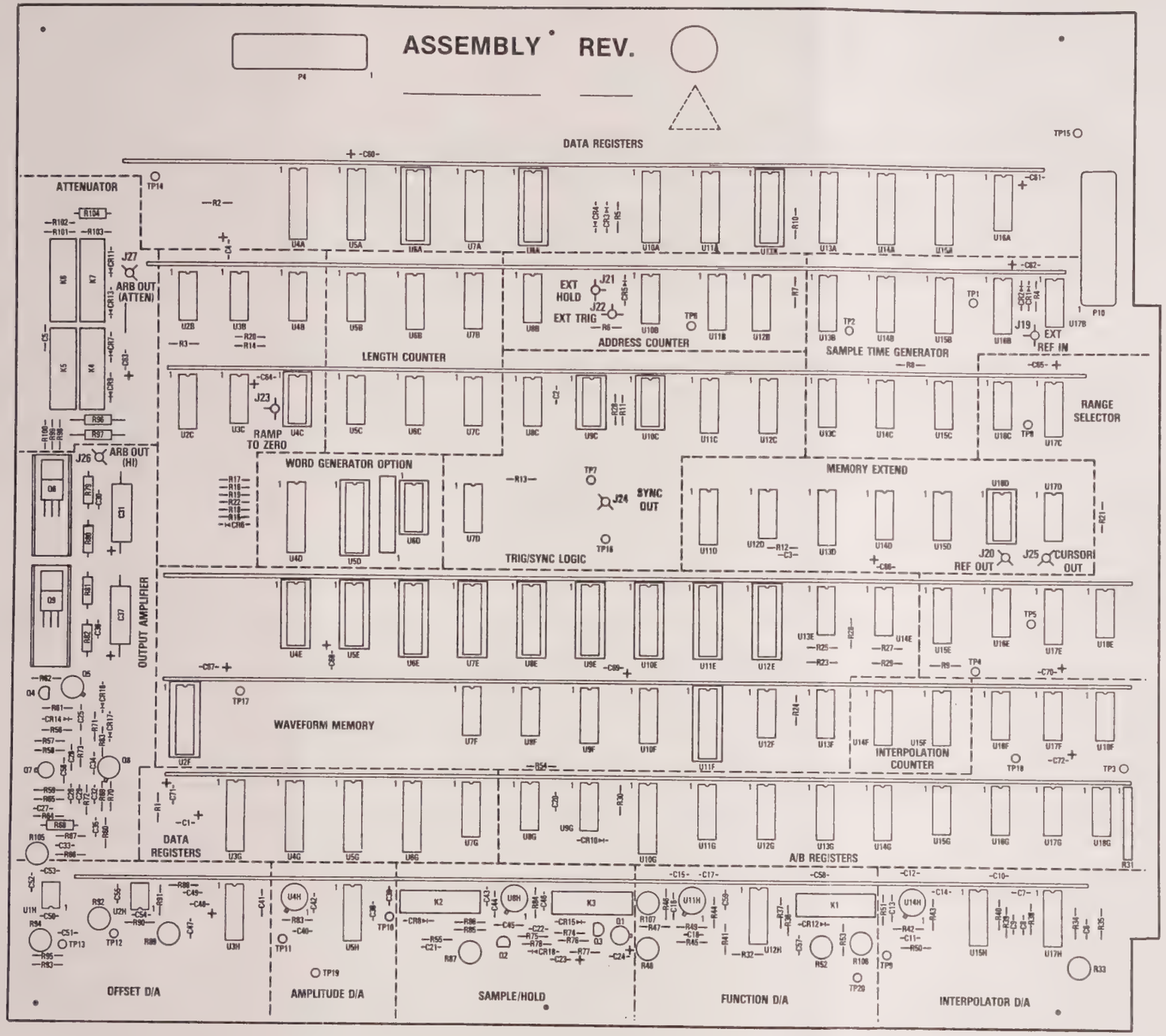

MADE FROM 0100-00-0644-3B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO
MATERIAL	PROJ ENGR		TITLE: ASSEMBLY, GENERATOR
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES ±1 XX .030		
	DO NOT SCALE DWG	MODEL 175	1100-00-0644 REV
	SCALE	DRAWING 23338	SHEET 1 OF 1

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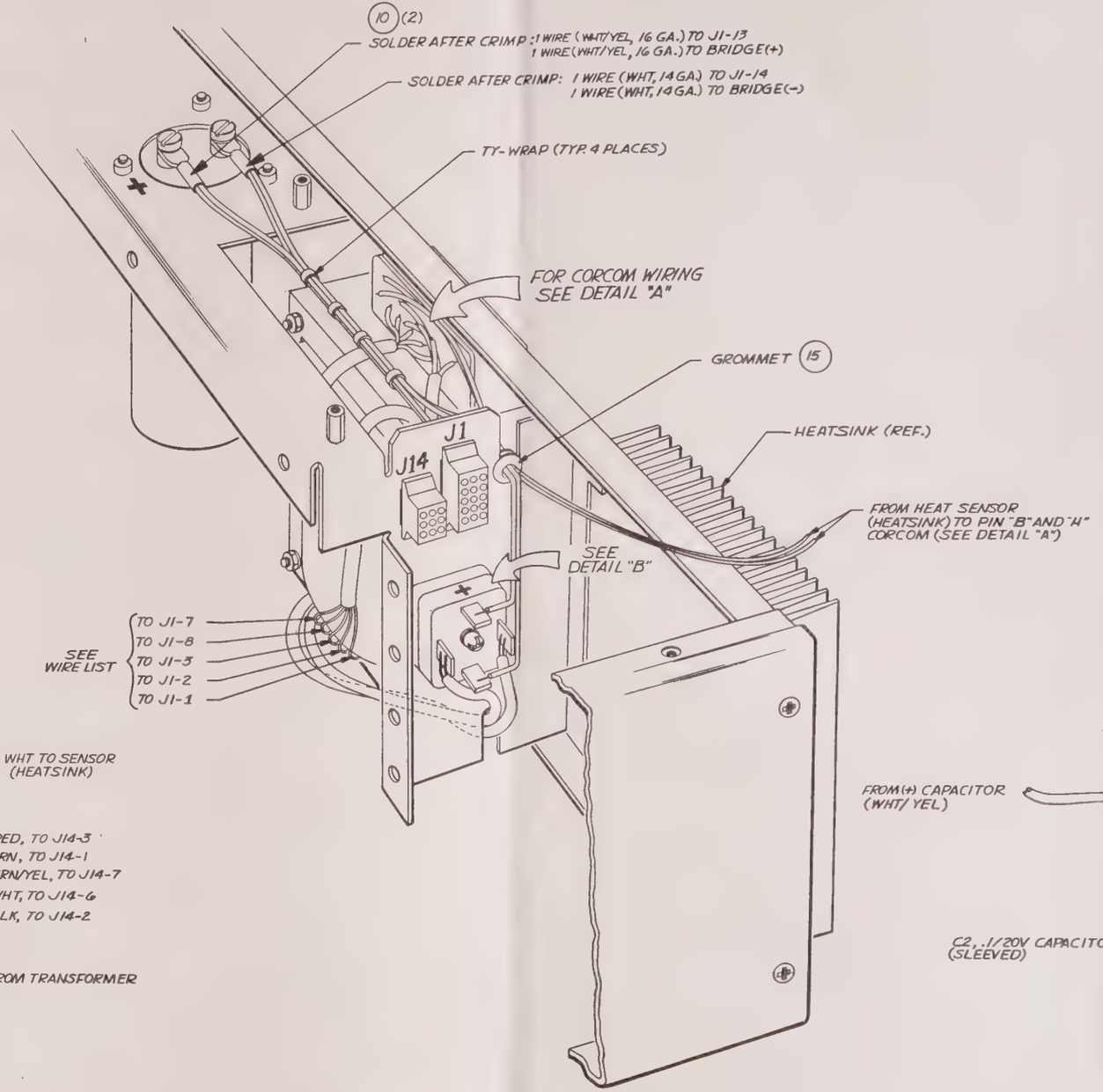
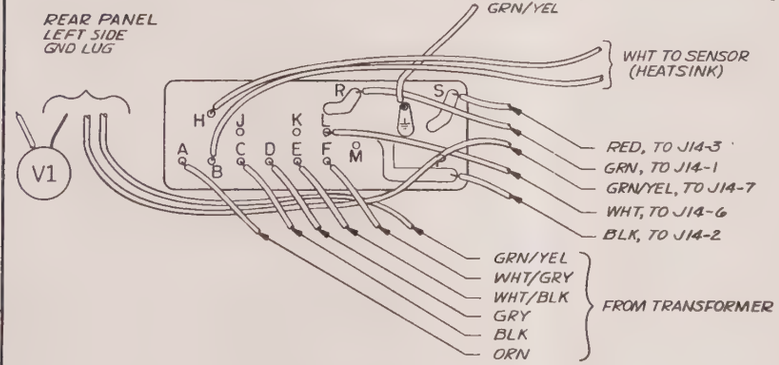
REV	ECN	BY	DATE	APP

WIRE LIST

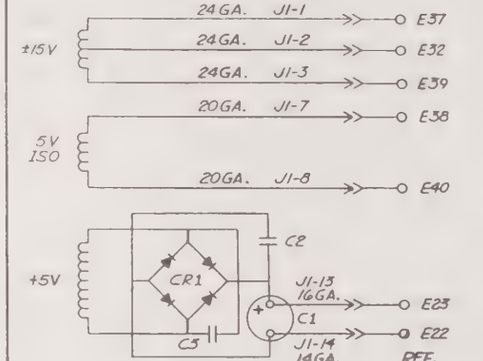
	PIN NO.	WIRE GA.	COLOR	FROM
J1 15 PIN MOLEX	1	24	RED	TRANSFORMER
	2	24	WHT/RED	"
	3	24	RED	TRANSFORMER
	4			NOT USED
	5			" "
	6			NOT USED
	7	20	BLU	TRANSFORMER
	8	20	BLU	TRANSFORMER
	9			NOT USED
	10			" "
	11			" "
	12			NOT USED
	13	16	WHT/YEL	CAPACITOR (+)
	14	14	WHT	CAPACITOR (-)
	15			NOT USED
J14 9 PIN MOLEX	1	20	GRN	CORCOM R
	2	20	BLK	CORCOM P
	3	20	RED	CORCOM S
	4 AND 5			NOT USED
	6	20	WHT	CORCOM L
	7	20	GRN/YEL	CORCOM (GND)
	8 AND 9			NOT USED

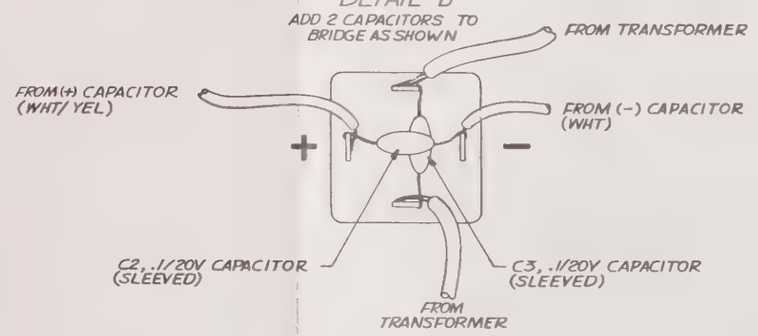

(10) (2)
SOLDER AFTER CRIMP: 1 WIRE (WHT/YEL, 16 GA.) TO J1-13
1 WIRE (WHT/YEL, 16 GA.) TO BRIDGE(+)
SOLDER AFTER CRIMP: 1 WIRE (WHT, 14 GA.) TO J1-14
1 WIRE (WHT, 14 GA.) TO BRIDGE(-)
TY-WRAP (TYP. 4 PLACES)
FOR CORCOM WIRING SEE DETAIL "A"
GROMMET (15)
HEATSINK (REF.)
FROM HEAT SENSOR (HEATSINK) TO PIN "B" AND "H" CORCOM (SEE DETAIL "A")
SEE DETAIL "B"
J1
J14
SEE WIRE LIST
TO J1-7
TO J1-8
TO J1-3
TO J1-2
TO J1-1



DETAIL "A"
CORCOM WIRING

SCHEMATIC





BNC DESTINATION

CURSOR OUT	TO	J25	MAIN BOARD	APPROX. LENGTH	31"
SYNC OUT	"	J24	" "	" "	24"
ARB OUT (HI)	"	J26	" "	" "	19"
ARB OUT (ATTEN)	"	J27	" "	" "	21"
RAMP TO ZERO	"	J23	" "	" "	19"
EXT HOLD	"	J21	" "	" "	27"
EXT TRIG	"	J22	" "	" "	27"
EXT REF	"	J19	" "	" "	34"
REF OUT	TO	J20	MAIN BOARD	APPROX. LENGTH	31"

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 5-5-78	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE ASSEMBLY REAR PANEL
FINISH WAVETEK PROCESS	RELEASE APPROV 6-9-78		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX .030		
	DO NOT SCALE DWG		MODEL NO 175
	SCALE		DWG NO. 0102-00-0667 REV E
			CODE IDENT 23338 SHEET 2 OF 2

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REV	ECN	BY	DATE	APP
B	ECN 1765	DA	10/	
C	ECN 1709	DA	8/	
D	ECN # 2276			
	2913 (CL III)		9/12	
	3247 (CL III)	DC		
	PLAN CLASS III			
E	# 7091 (CLASS II)	M.C. 3-5-87		

NO. 4-40 x 3/8" FLAT HEAD SCREW (5)

CAP. BRACKET MTG., USE NO. 6-32 x 3/8" PAN HEAD SCREW WITH SPLIT LOCK WASHER (4)

(8) NO. 6-32 x 3/8" SOCKET HEAD CAP SCREW GND. LUG, SPLIT LOCK WASHER AND CASTLE NUT (APPLY LOCK-TITE) (2)

SHOULDER WASHER
NYLON FLAT WASHER
SOLDER LUG
INTERNAL TOOTH LOCK WASHER
NUT

(7) (9) (18) TYP. BNC HARDWARE STACK-UP (9 USED)

T1 MOUNTING, NO. 10-32 x 1¾ PAN HEAD SCREW WITH SPLIT LOCK WASHER, FLAT WASHER AND NUT (3 PLCS. ONLY)

CORCOM IS SELF RETAINING

S1 WITH "F1"

HEATSINK (REF.)

(17) (2) NOT SHOWN FOR CLARITY

(5) (11)

(4)

(6)

NO. 10-32 x 1¾" PAN HEAD SCREW (THIS LOCATION ONLY)

V1 SLEEVED

T1

(7) (12)

USE LOC-TITE (4 PLCS.)

(2)
(1)

(3)
(14)

APPLY THERMAL COMPOUND PRIOR TO INSTALLATION

BRACKET (T1 MTG.) WITH NO. 10 PRESS NUT

NO. 6-32 x 3/8" PAN HEAD SCREW WITH SPLIT LOCK WASHER (4)

(16)

*8 PRESS NUT (13)

NO. 6-32 x 3/8" PAN HEAD SCREW WITH SPLIT LOCK WASHER, FLAT WASHER AND PRESS NUT (3 PLCS.) (APPLY LOC-TITE)

C1

BRACKET RIVET (2)

NO. 8-32 x ¾" PAN HEAD SCREW WITH SPLIT LOCK WASHER

CR1

(19) WRAP STRIP BETWEEN CAPACITOR AND BRACKET

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 5278	WAVETEK SAN DIEGO, CA
MATERIAL	PROJ ENGR		TITLE ASSEMBLY REAR PANEL
FINISH WAVETEK PROCESS	RELEASE APPROV 6 9 77		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 XX ± .030 ANGLES ±1°		
	DO NOT SCALE DWG		
	SCALE	MODEL NO 175	DWG NO. 0102-00-0667 REV E
		CODE IDENT 23338	SHEET 1 OF 2

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, HEATSINK	0102-00-0668	WVTK	0102-00-0668	1
NONE	SCHEMATIC, PWR SUPPLY	0103-00-0659	WVTK	0103-00-0659	1
1	HEATSINK REF: 3200-06-0011	175-8403	WVTK	1400-00-8403	1
C10	CAP CER MON .01MF 50V, AXIAL	CAC02Z5U103Z100A	CORNG	1500-01-0310	1
J16	CONN, 15PIN	03-09-1151	MOLEX	2100-02-0012	1
NONE	PIN, FEMALE	350417-1	AMP	2100-05-0026	12
NONE	CONNECTOR PIN	350415-1	AMP	2100-05-0039	3
NONE	TIE STRAP	SST-1.5M	PANDT	2800-00-0003	4
3	CABLE CLAMP	E-3	RICH	2800-00-0009	1
2	CABLE CLAMP	770-1505	CONCD	2800-00-0010	1
4	RETAINER, SPRING	D3BE1910Y	BRADY	2800-09-0007	1
NONE	WASHER	B51547F015	MOT	2800-11-0015	6
NONE	INSULATOR(TO-220)	60-11-8302-1674	CHOMR	3100-00-0010	5
R1	RES, WW, 10W, 3%, .1 OHM	RH10-.1 OHM 3%	DALE	4702-77-0019	1
Q7	TRANS	2N6486	MOT	4901-06-4860	1
Q1 Q14	TRANS	2N6489	MOT	4901-06-4890	2

WAVETEK PARTS LIST | TITLE: HEATSINK | ASSEMBLY NO. 1101-00-0668 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CR24	TRANS	2N6504	MOT	4901-06-5040	1
Q2	TRANS	TIP-36	TI	4902-00-0360	1
F2	THERMOSTAT (180°F/83°C)	3450-22-110/T101	ELMWD	5300-00-0003	1
Q18	VOLT REG	MA7805UC	FAIR	8000-78-0500	1

WAVETEK PARTS LIST | TITLE: HEATSINK | ASSEMBLY NO 1101-00-0668 | REV C

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST HEATSINK
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 175	DWG NO 1101-00-0668 REV C
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS RECORDER NO. A-3894

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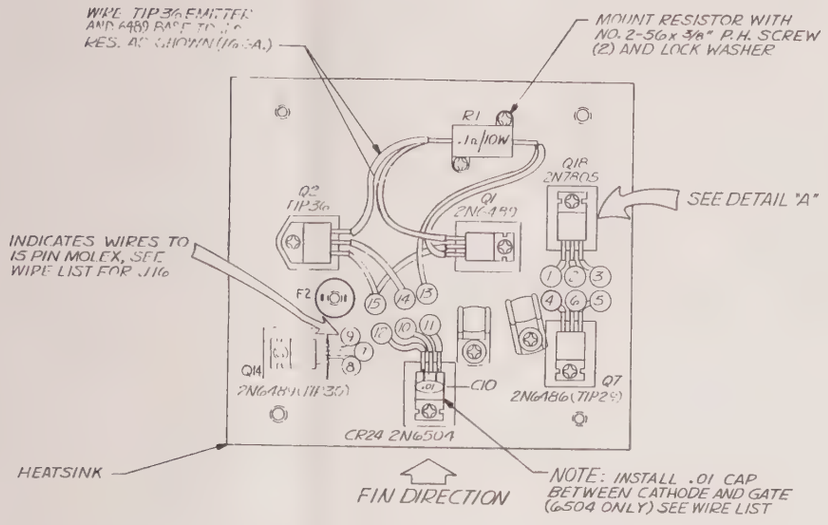
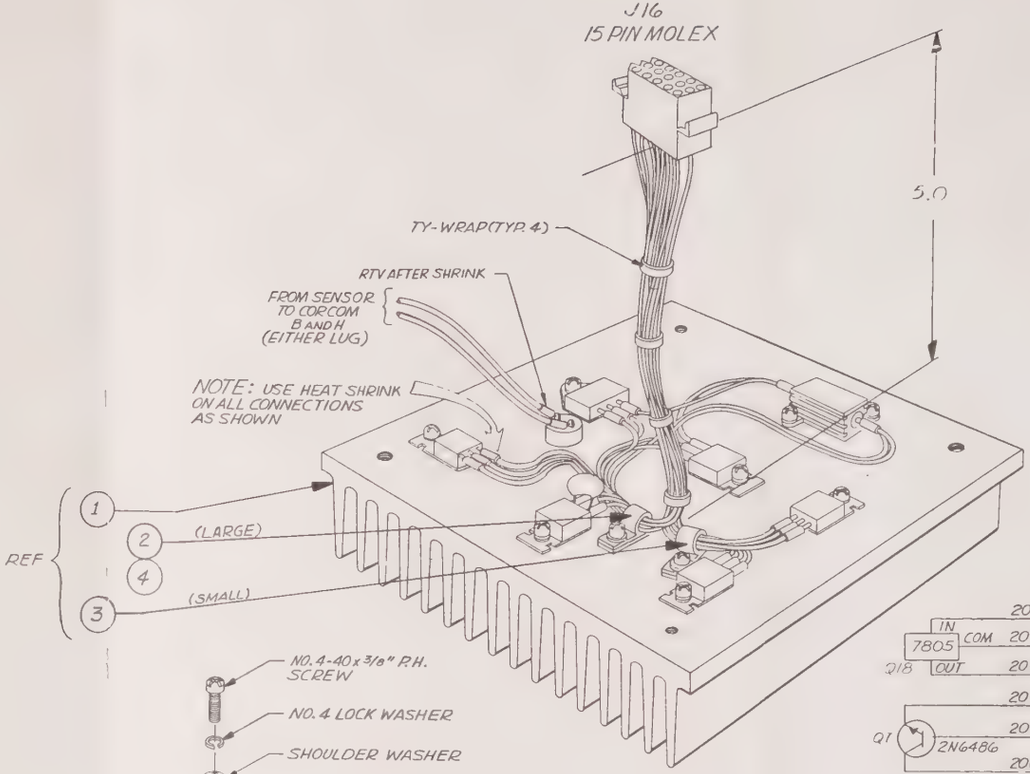
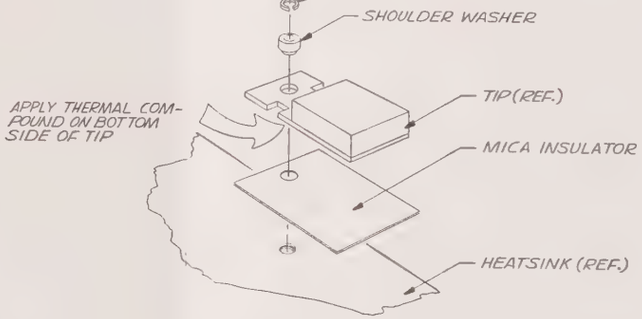
REV	ECN	BY	DATE	APP
B	1814	[illegible]	[illegible]	
C	3023	[illegible]	[illegible]	
D	3479	[illegible]	[illegible]	
E	7980	[illegible]	[illegible]	

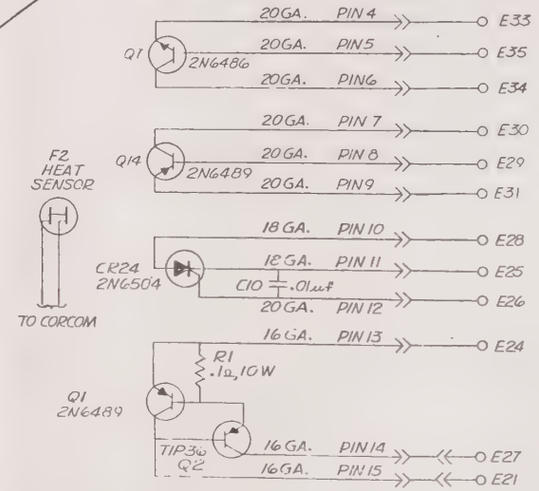

WIRE TIP36 EMITTER AND 6489 BASE TO R1 RES. AS SHOWN (J16-A.)
MOUNT RESISTOR WITH NO. 2-56 x 3/8" P.H. SCREW (2) AND LOCK WASHER
R1 .1Ω 10W
Q18 2N7805
Q2 TIP36
Q1 2N6489
SEE DETAIL "A"
INDICATES WIRES TO 15 PIN MOLEX, SEE WIRE LIST FOR J16
F2
Q14 2N6489 (TIP30)
C10
Q7 2N6486 (TIP29)
CR24 2N6504
HEATSINK
FIN DIRECTION
NOTE: INSTALL .01 CAP BETWEEN CATHODE AND GATE (6504 ONLY) SEE WIRE LIST





DETAIL "A"
TIP INSTALLATION (TYP. 6)

SCHEMATIC



WIRE LIST "J16"

PIN NO.	WIRE GA.	COLOR	FROM
1	20GA	WHT	7805 "IN"
2	20GA	WHT	7805 "COM"
3	20GA	WHT	7805 "OUT"
4	20GA	WHT	6486 (TIP29) EMITTER
5	20GA	WHT	6486 (TIP29) BASE
6	20GA	WHT	6486 (TIP29) COLLECTOR
7	20GA	WHT	6489 (TIP30) COLLECTOR
8	20GA	WHT	6489 (TIP30) BASE
9	20GA	WHT	6489 (TIP30) EMITTER
10	18GA	WHT	6504 ANODE
11	18GA	WHT	6504 CATHODE — .01/50V
12	20GA	WHT	6504 GATE — .01/50V
13	16GA	WHT	.1Ω RES.
14	16GA	WHT	TIP36 COLLECTOR
15	16GA	WHT	TIP36 BASE, 6489 COLLECTOR

1. APPLY THERMAL COMPOUND ON BASE OF ALL COMPONENTS.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 4-78	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE ASSEMBLY HEAT SINK
FINISH WAVETEK PROCESS	RELEASE APPROV [illegible] 5-9-78		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1° XX ± .030		
	DO NOT SCALE DWG		MODEL NO. 175
	SCALE		DWG NO 0102-00-0666 REV D
			CODE IDENT 23338 SHEET 1 OF 1

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	ASSY DRWG, PWR SUPPLY	0101-00-0659	WVTK	0101-00-0659	1
NONE	SCHEMATIC, PWR SUPPLY	0103-00-0659	WVTK	0103-00-0659	1
2	BRACKET, ANGLE	175-8453	WVTK	1400-00-8453	1
C5	CAP, CER, .001MF, 1KV	DD-102	CRL	1500-01-0211	1
C14 C16 C17 C18 C19 C20 C23 C24 C26 C6	CAP, CER, MN, .01MF, 50V	GE30-103ZA	MURAT	1500-01-0310	10
C21 C27 C34 C36 C50 C8	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z050A	CORNG	1500-01-0405	6
C7	CAP, CER, 470PF, 1KV	DD-471	CRL	1500-04-7111	1
C22 C28 C37	CAP, ELECT, 100MF, 16V	500D1070016DC7	SPRAG	1500-31-0101	3
C15 C25	CAP, ELECT, 1000MF, 35V	39D10BG035GL6	SPRAG	1500-31-0212	2
C9	CAP, ELECT, 1900MF, 15V	39D19BG015GL4	SPRAG	1500-31-9201	1
C35	CAP, ELECT, 4000MF, 15V	TCG402U015N1L	MAL	1500-34-0211	1
C49	CAP, TANT, 5.6MF, 35V	150D565X9035B2	SPRAG	1500-75-6302	1
1	POWER SUPPLY BOARD	175-0659	WVTK	1700-00-0659	1
P1 P16	PLUG, 15PIN	03-09-2151	MOLEX	2100-02-0013	2
NONE	PIN, MALE	350148-1	AMP	2100-05-0005	22
NONE	CONNECTOR PIN(16/14)	350416-1	AMP	2100-05-0040	5

WAVETEK PARTS LIST | TITLE: PCA, POWER SUPPLY | ASSEMBLY NO. 1100-00-0659 | REV E | PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R3	RES, MF, 1/8W, 1%, 511	RN55D-5110F	TRW	4701-03-5110	1
R10 R27	RES, MF, 1/8W, 1%, 5.76K	RN55D-5761F	TRW	4701-03-5761	2
R24	RES, MF, 1/8W, 1%, 8.25K	RN55D-8251F	TRW	4701-03-8251	1
R2	RES, WW, 5W, 10%, 10	PW-5	TRW	4702-66-0100	1
R35 R37	RES, SET, 2-10K, 1/8W QTY: 2: 4701-03-1002	142-501-64A	WVTK	4709-00-0019	1
CR11	DIODE	1N4581	MICRO	4801-01-4581	1
CR10 CR15 CR16 CR17 CR18 CR7 CR8 CR9	DIODE	1N4002	FAIR	4801-02-0001	8
CR5	DIODE	1N4148	FAIR	4807-02-6666	1
Q8	TRANS	2N2219A	NEC	4901-02-2191	1
Q13	TRANS	2N2905A	NEC	4901-02-9031	1
Q11 Q12	TRANS	2N3638A	CARTR	4901-03-6381	2
Q10 Q9	TRANS	2N3642	FAIR	4901-03-6420	2
Q3	TRANS	2N6486	MOT	4901-06-4860	1
U1 U3 U4	IC	LM741CN	NSC	7000-07-4100	3
U2	IC	MC 3423	MOT	7000-34-2300	1

WAVETEK PARTS LIST | TITLE: PCA, POWER SUPPLY | ASSEMBLY NO. 1100-00-0659 | REV E | PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
J4 J5 J6	HEADER, 34 PIN	929836-01-17	AP	2100-05-0041	3
NONE	TIE STRAP	SST-1.5M	PANDT	2800-00-0003	18
NONE	GROMMET, RUBBER	2177	SMITH	2800-10-0005	1
4	TRANSIPAD	10160	METRS	2800-11-0004	2
3	SCREW, CAPTIVE	DKN7900-6A2	DUTCH	2800-23-0010	1
R26	POT, TRIM, 1K	91AR1K	BECK	4600-01-0209	1
R17 R38	RES, C, 1/2W, 5%, 2.7	RC-1/2-2R7J	STKPL	4700-25-0279	2
R22 R23 R30 R34	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	4
R6	RES, MF, 1/8W, 1%, 12.1K	RN55D-1212F	TRW	4701-03-1212	1
R11	RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	1
R18 R36	RES, MF, 1/8W, 1%, 215	RN55D-2150F	TRW	4701-03-2150	2
R28	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	1
R4	RES, MF, 1/8W, 1%, 274	RN55D-2740F	TRW	4701-03-2740	1
R20 R33 R5 R8	RES, MF, 1/8W, 1%, 3.01K	RN55D-3011F	TRW	4701-03-3011	4
R21 R29	RES, MF, 1/8W, 1%, 4.64K	RN55D-4641F	TRW	4701-03-4641	2
R19 R32	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	2
R25 R31 R9	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	3

WAVETEK PARTS LIST | TITLE: PCA, POWER SUPPLY | ASSEMBLY NO. 1100-00-0659 | REV E | PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT

WAVETEK PARTS LIST | TITLE: PCA, POWER SUPPLY | ASSEMBLY NO. 1100-00-0659 | REV E | PAGE 4

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: PARTS LIST PCA, POWER SUPPLY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 175 / DWG NO 1100-00-0659 / REV E
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

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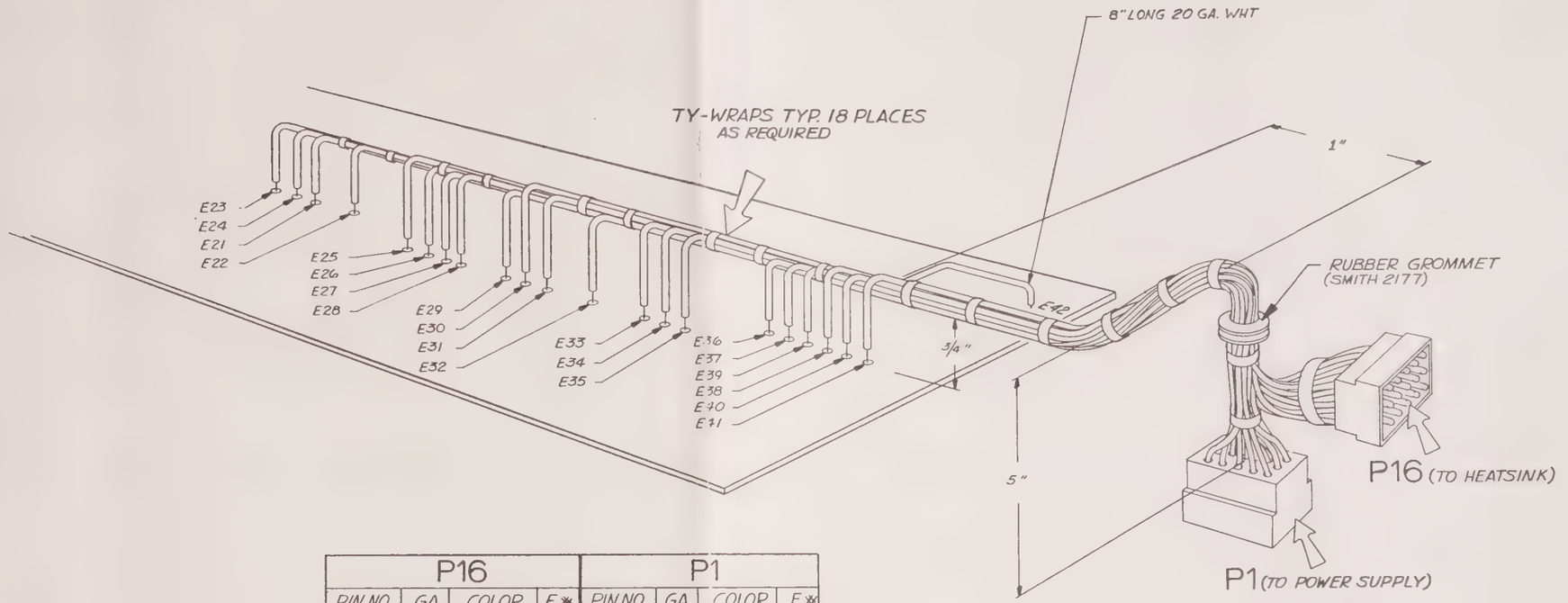
REV	ECN	BY	DATE	APP



P16				P1			
PIN NO.	GA.	COLOR	E #	PIN NO.	GA.	COLOR	E #
1	20	WHT	41	1	20	WHT	37
2			42	2	20	WHT	32
3			36	3	20	WHT	39
4			33	4		NOT USED	
5			35	5		NOT USED	
6			34	6		NOT USED	
7			30	7	20	WHT	38
8			29	8	20	WHT	40
9	20		31	9		NOT USED	
10	18		28	10		NOT USED	
11	18		25	11		NOT USED	
12	20		26	12		NOT USED	
13	16		24	13	16	WHT	23
14	16		27	14	14	WHT	22
15	16	WHT	21	15		NOT USED	

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 5-9-78	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE ASSEMBLY POWER SUPPLY
FINISH WAVETEK PROCESS	RELEASE APPROV 6-9-78		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG		MODEL NO 175 / DWG NO 0101-00-0659 / REV E
	SCALE		CODE IDENT 23338

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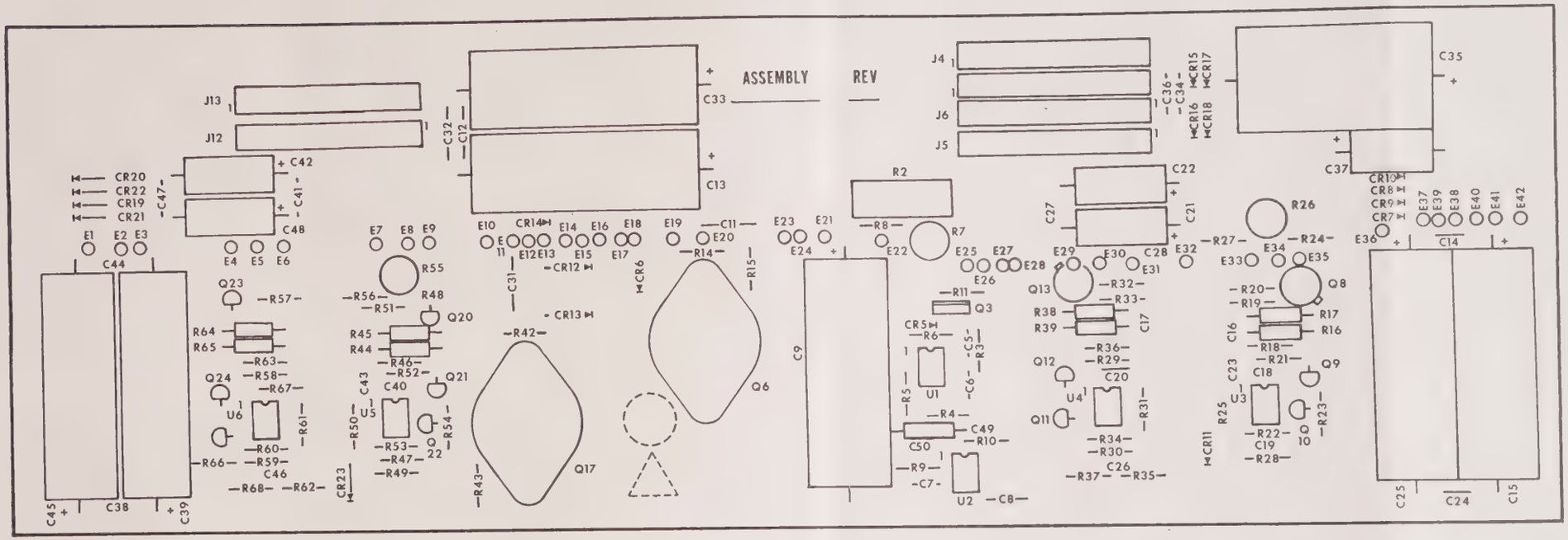

CREATED FROM 0100-00-0659-3C

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE ASSEMBLY POWER SUPPLY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES ±1 XX .030		
	DO NOT SCALE DWG		MODEL NO 175 / DWG NO 1100-00-0659 / REV
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

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REV	ECN	BY	DATE	APP
C	...16			

OVER VOLTAGE PROTECT

CR14 1N6504 C10 .01 J1612 J116-11 J116-10 P1612 E26 P1611 P1610 E25 E28

T1 SHIELD GRN/YEL GND CHASSIS

HOT PHASE
SAFETY GND
NEUT PHASE

S1 P15-3 J15-3 P14-3 J14-3 BLU BRN OFF ON GRN/YEL WHT/BRN WHT/BLU

CORCOM 6J1 S1

F1 F2 THERMAL CUTOFF

WHT/GRY

FRONT PANEL | REAR PANEL

BLK ORN BLK/WHT GRY

J1-13 P1-13 E23 E24 P16-13 J116-13 R1 .1Ω,10W J116-14 P16-14 E27 Q2 TIP-36 J16-15 Q1 2N6489 P16-15 E21 R2 10Ω,5W Q3 2N6486

C5 .001 C6 .01 +15V R4 274Ω R11 2K R3 511Ω U1 μA741 -15V R5 3.01K R6 12.1K +15V R8 3.01K CR5 FD6666

R10 5.76K R9 4.99K C7 470PF MC 3423 U2 C49 5.6μf C50 .1/20 C8 .1/20 C9 1900 μf,15V

J4,5,6 +5V 6AMP MAX (PINS 1-6)

+5V COM (PINS 7-18, 20, 23, 24, 28, 31, 32 25,& 27)

J1-14 P1-14 E22 COM

J1-7 P1-7 E38 J1-8 P1-8 E40 CR15 SCE-1(4) CR16 CR17 CR18

C34 .1/20 C35 4000μf 15V

E41 P16-1 J116-1 Q18 7805 IN OUT COM J116-3 P16-3 E36 J116-2 P16-2 E42

C36 .1/20 C37 100μf 16V

ISO +5V 0.75AMP MAX (PINS 29, 30)

ISO +5V COM (PINS 33, 34)

J1-1 P1-1 E37 J1-2 P1-2 E32 J1-3 P1-3 E39 CR7 SCE-1(4) CR8 CR9 CR10

Q7 (TIP29) 2N6486 J116-6 J116-5 J116-4 P16-6 P16-5 P16-4 TBD R16 E34 E35 E33 R17 2.7Ω,½W

+15V 0.5AMP MAX (PIN 26)

C14 .01 C15 1000μf 35V R19 499Ω R20 3.01K Q8 2N2219A 10123N C16 .01 R21 4.64K R18 215Ω Q9 2N3642 (2) Q10 R22 1K R23 1K

C18 .01 U3 μA741 TRIM R26 1K C19 .01 -15V R24 8.24K R25 4.99K R27 5.76K CR11 IN4581 R28 2.49K C21 .1μf 20V C22 100μf 16V C23 .01

±15V COM (PINS 21, 22)

C24 .01 C25 1000μf 35V C17 .01 R32 499Ω R33 3.01K Q13 2N2905A 10123N R29 4.64K R30 1K Q11 2N3638A (2) Q12 R34 1K

C20 .01 +15V U4 μA741 C26 .01 R31 4.99K +15V R35 10K* R37 10K* C27 .1μf,20 C28 100μf 16V

R36 215Ω R38 2.7Ω,½W R39 TBD E30 E29 E31 P16-7 P16-8 P16-9 J16-7 J16-8 J16-9 Q14 (TIP30) 2N6489

-15V 0.5AMP MAX (PIN 19)

LAST DES USED:

C50	S1
F2	T1
U6	CR24
RL8	Q26

4. RESISTORS ARE ⅛ W, 1%, M.F.
3. – – – – = HEATSINK
2. * = MATCHED SET OF 10K
1. ALL CAPACITANCE IN MICROFARADS

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN J.D. COOPER	DATE 1-16-78	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE SCHEMATIC POWER SUPPLY
FINISH WAVETEK PROCESS	RELEASE APPROV		
DO NOT SCALE DWG	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
SCALE	MODEL NO 175	DWG NO 0103-00-0659	REV C
	CODE IDENT 23338	SHEET / OF /	

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R57	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	1
R20 R21 R22 R23 R24 R29 R33 R50 R62 R69	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	10
R30 R34 R42 R48 R49 R71	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	6
R66	RES, MF, 1/8W, 1%, 1.21K	RN55D-1211F	TRW	4701-03-1211	1
R56	RES, MF, 1/8W, 1%, 15K	RN55D-1502F	TRW	4701-03-1502	1
R31 R32 R45 R47 R51 R70	RES, MF, 1/8W, 1%, 182	RN55D-1820F	TRW	4701-03-1820	6
R53 R54 R65 R68	RES, MF, 1/8W, 1%, 1.96K	RN55D-1961F	TRW	4701-03-1961	4
R64	RES, MF, 1/8W, 1%, 2.21K	RN55D-2211F	TRW	4701-03-2211	1
R4	RES, MF, 1/8W, 1%, 274	RN55D-2740F	TRW	4701-03-2740	1
R1	RES, MF, 1/8W, 1%, 30.1K	RN55D-3012F	TRW	4701-03-3012	1
R12	RES, MF, 1/8W, 1%, 4.87K	RN55D-4871F	TRW	4701-03-4871	1
R74 R75	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	2
R27 R28 R3 R35 R46 R58 R59 R60	RES, MF, 1/8W, 1%, 6.81K	RN55D-6811F	TRW	4701-03-6811	8
R37 R38 R39 R40 R41 R43 R44 R52	RES, MF, 1/8W, 1%, 750	RN55D-7500F	TRW	4701-03-7500	8
R2	RES MODULE, 10K	4310R-101-103	BOURN	4770-00-0008	1

WAVETEK PARTS LIST | TITLE: PCA, M-PROC/GPIB BD | ASSEMBLY NO. 1100-00-0660 | REV K | PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	ASSY DRWG, GPIB/MPROC	0101-00-0660	WVTK	0101-00-0660	1
NONE	SCHEMATIC, GPIB/MPROC	0103-00-0660	WVTK	0103-00-0660	1
T1	TRANSFORMER	175-0024	WVTK	1204-00-0024	1
1	CONN. BLOCK	157-314	WVTK	1400-00-3043	2
2	BLOCK, JACK SCREW	178-8473	WVTK	1400-00-8473	2
C37	CAP, CER, 100PF, 1KV	DD-101	CRL	1500-01-0111	1
C10 C11 C12 C13 C14 C15 C16 C17 C33 C34 C39 C40 C41 C6 C7 C8 C9	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z050A	CORNG	1500-01-0405	17
C18	CAP, CER, 22PF, 1KV	DD-220	CRL	1500-02-2011	1
C36 C38	CAP, CER, 220PF, 1KV	DD-221	CRL	1500-02-2111	2
C35	CAP, MICA, 1000PF, 500V	DM15-102J	ARCO	1500-11-0200	1
C1 C2 C3 C4 C5	CAP, TANT, 33MF, 10V	150D336X9010B2	SPRAG	1500-73-3601	5
3	GPIB/MPROC BOARD	175-0660	WVTK	1700-00-0660	1
J17	CONN	57-20240	AMPH	2100-02-0060	1
NONE	SKT, IC, 16PIN	DILB-16P-108	BURND	2100-03-0028	6
NONE	SKT, IC, 40PIN	DILB-40P-108	BURND	2100-03-0030	3
NONE	SOCKET	516-AG7D	AUGAT	2100-03-0034	1

WAVETEK PARTS LIST | TITLE: PCA, M-PROC/GPIB BD | ASSEMBLY NO 1100-00-0660 | REV K | PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
U18D	TTL, NAND, QUAD 2INP	74LS00	TI	8000-74-0010	1
U11B U5C	TTL, INVERTER, HEX	74LS04	TI	8000-74-0410	2
U19D2	IC, HEX INVERTER, LOW POWER SCHOTTKY	SN74LS04N	MOT	8000-74-0411	1
U5B	IC	7405	TI	8000-74-0500	1
U11C U9D	TTL, AND, QUAD 2INP	74LS08	TI	8000-74-0810	2
U9B	TTL, AND, 3INP	74LS11	TI	8000-74-1110	1
U10B	TTL, OR, QUAD 2INP	74LS32	TI	8000-74-3210	1
U8C	TTL, NAND, QUAD 2INP	74LS38	TI	8000-74-3810	1
U10C U4D1 U4D2 U5D1 U5D2 U8B U9A	TTL, D-F/F, DUAL	74LS74	TI	8000-74-7410	7
U9C	CMOS, SHFT REG, 188 BT	MC14006BCP	MOT	8001-40-0600	1
U10D U6C	TTL, NAND, QUAD S/TRIG	74LS132	TI	8007-41-3210	2
U20C U20D	TTL, DCDR, 3-8 LINE	74LS138	TI	8007-41-3810	2
U19D1	TTL, CNT, SYNC 4B	74LS161	BIO	8007-41-6110	1
U12C U13C U14C U4A U6A	TTL, BUF, OCT, 3 ST OUT	74LS244	TI	8007-42-4410	5
U10A	TTL, XCVR, OCT BUS	74LS245	TI	8007-42-4510	1
U3A U3B	TTL, XNOR, QUAD 2INP	74LS266	TI	8007-42-6610	2

WAVETEK PARTS LIST | TITLE: PCA, M-PROC/GPIB BD | ASSEMBLY NO 1100-00-0660 | REV K | PAGE 5

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R61 R63 R67	RES MODULE 2.2K	4310R-101-222	BOURN	4770-00-0011	3
R25 R26 R36	RES MODULE	4310R-101-682	BOURN	4770-00-0016	3
CR1 CR15 CR2 CR3 CR4 CR5 CR6 CR7	DIODE	1N4148	FAIR	4807-02-6666	8
Q8	TRANS	2N3903	NSC	4901-03-9030	1
SW1	SWITCH PC	500-105	DUNCN	5199-00-0001	1
9	BUSS WIRE, 22GA	298	ALPHA	6000-92-2000	1
P5	ASSY, RIBBON CABLE	922522-34-02-13	AP	6002-00-0008	1
10	POWER BUSS BAR (LG)	6009-90-0004	WVTK	6009-90-0004	1
U1A1 U1A2 U1A3 U2A1 U2A2 U7A2 U7D1 U8A2	OPTO-COUPLER	4N26	MOT	7000-04-2600	8
U6B U7A1 U7C U7D2 U8A1 U8D	OPTO CPLR, FAST	6N136	SPECT	7100-00-0001	6
U18C1 U19C1	MOS, RAM, 1KX4	UPD2114LC	NEC	8000-21-1400	2
U12D	IC	2650	BIO	8000-26-5000	1
U1B U1C U2B U2C	XCVR, QUAD BUS	MC3446P	MOT	8000-34-4600	4
U6D	CMOS, QUAD NAND S/TRG	CD4093BE	RCA	8000-40-9300	1
U16D U3C	CMOS, UART	IM6402CPL	INTSL	8000-64-0200	2

WAVETEK PARTS LIST | TITLE: PCA, M-PROC/GPIB BD | ASSEMBLY NO. 1100-00-0660 | REV K | PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	SOCKET, 18 PIN	DIBL-18P-108	BURND	2100-03-0050	2
NONE	SOCKET, 20 PIN	DIBL-20P-108	BURND	2100-03-0051	1
U12A	SOCKET, IC, 28 PIN	DILB28P-108T	BURND	2100-03-0081	1
NONE	PIN, MALE	60809-2	AMP	2100-05-0020	10
J10 J11	HEADER, 34 PIN	929836-01-17	AP	2100-05-0041	2
Y1	CRYSTAL, 10MHZ	590-302	WVTK	2300-99-0006	1
4	JACK SCREW	408-146475	AMPH	2800-23-0008	2
6	SCREW, PAN STAINLESS STEEL, 18-8, 4-40 X 3/8	2800-23-4106	WVTK	2800-23-4106	8
5	WASHER, SPLIT LOCK, 4	#4SRLW	CMRCL	2800-42-4000	2
NONE	LOCKWASHER, #8 SPLIT RING BIN 340	#8SRLW	CMRCL	2800-42-8000	2
U11A	SHUNT	435704-B	AMP	3000-00-0033	1
NONE	JUMPER	461-2871-01-03-10	CAMB	3000-00-0034	1
NONE	PINS, JUMPER	450-3704-01-03	CAMB	3000-00-0035	4
R77 R78	RES, CAR, 1/8W, 5%, 4.7K	RC05GF472J	AB	4700-05-4701	2
R55 R72 R73	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	3

WAVETEK PARTS LIST | TITLE: PCA, M-PROC/GPIB BD | ASSEMBLY NO. 1100-00-0660 | REV K | PAGE 2

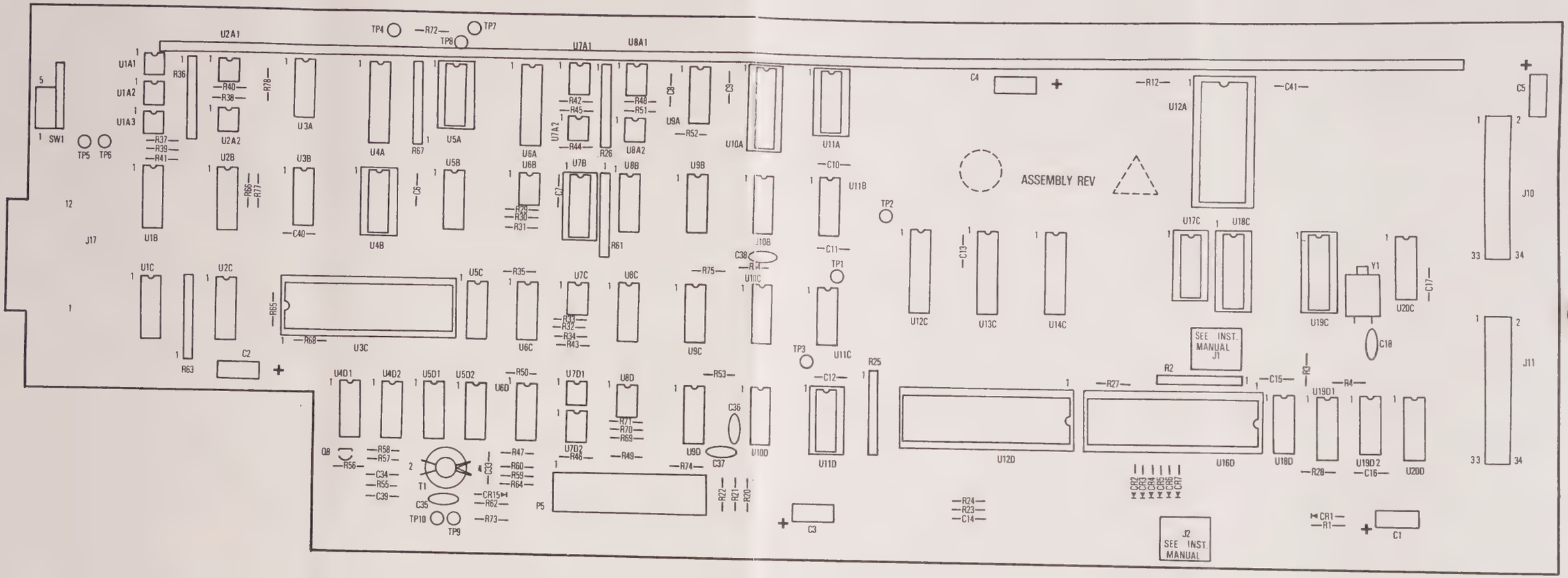
REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
U7B	IC, PROGRAMMED REF: 8007-41-8801	8600-00-0091	WVTK	8600-00-0091	1
U5A	IC, PROGRAMMED REF: 8007-41-8801	8600-00-0092	WVTK	8600-00-0092	1
U4B	IC, PROGRAMMED REF: 8008-21-2601	8600-00-0093	WVTK	8600-00-0093	1
U11D	IC, PROGRAMMED REF: 8007-41-8801	8600-00-0147	WVTK	8600-00-0147	1
NONE	IC, PROGRAMMED REF: 8000-27-6400	8600-00-0299	WVTK	8600-00-0299	1
U17C	IC, PROGRAMMED REF: 8007-41-8801	8600-00-0300	WVTK	8600-00-0300	1

WAVETEK PARTS LIST | TITLE: PCA, M-PROC/GPIB BD | ASSEMBLY NO. 1100-00-0660 | REV K | PAGE 6

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: PARTS LIST PCA, M-PROC/GPIB BD
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 175 / DWG NO 1100-00-0660 / REV K
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3804



MADE FROM 0100-00-0660-3C

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: ASSEMBLY, MICROPROCESSOR/GPIB
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 175 · DWG NO 1100-00-0660 · REV
	SCALE		CODE IDENT 23338 · SHEET 1 OF 1

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REV	ECN	BY	DATE	APP

NOTE UNLESS OTHERWISE SPECIFIED
1. + = 5V ISO

LAST USED:
C40 SW1
CR15 TP10
J17 U20D
R78 Y1
Q8

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 1-6-78	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR K. T.		TITLE SCHEMATIC GPIB MICRO PROC
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 175
	SCALE		DWG NO 6103-00-0660 REV K
			CODE IDENT 23338 SHEET 2 OF 2

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REV	ECN	BY	DATE	APP
B	ECN UPDATE	TLF	2-14-78	
D	ECN 1761	RO	7-27-78	

POWER SUPPLY P5

+5V COM
-15V
+5V COM
±15V
COM
+5V COM
+15V
+5V COM
+5V ISO
+5V COM
+5V ISO COM

* = NOT USED

C3 33/10V

BR/W → U11C LS08 → WEA
BWPP → U18D LS00 → WE/PAM

74S188 U17C MEM DECODER
A10 A11 A12 A13 A14
PR0
R12 4.87K
R3 6.81K
PAM
MOP
J1 (NORM CLOSED)

C11 .1/50V
U18D LS00 → IOP
BOPREQ
BM/IO
U10D LS132 → MOP
10MHz

C18 22pf
Y1 XTAL 10MHz
R4 274Ω
C16 .1/50V
U19D2 LS04

RESET
C1 33/10V
CR1 6666
30.1K R1
5V
U10D LS132 → MRSET

BUFFER LS244(3)
C13 .1/50V
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12
E/NE (A13)
D/C (A14)
BOPREQ
BM/IO
BR/W
BWRP
BFLAG
WE ANALOG
WE DISPLAY
U12C U13C U14C
U12D µP 2650
1.25MHz

R2 10K ×8 → DBUS0 DBUS1 DBUS2 DBUS3 DBUS4 DBUS5 DBUS6 DBUS7
C14 .1/50V
CR2 CR3 CR4 CR5 CR6 CR7 6666(6)
J2 (NORM OPEN)

U11B LS04
R20 10K → ADREN
R21 10K → DBUSEN
R22 10K → OPACK
R25 6.8K R24 10K R23 10K

U19D1 74LS161
U19D2 LS04 → 5MHz, 1.25MHz

C12 .1/50V
(A14) D/C
(A13) E/NE
BR/W
BM/IO
RAM
U11D 74S188 I/O DECODER
BOPREQ
U11B LS04

R25 6.8K SIP
RDATA WDATA RCONT DIRECT REXT WEXT ANAMEM BUFEN

WRITE EXTENDED DECODER U20C 74LS138
A4 A5 A6 A7
WEXT
C17 .1/50V
WBNK0 WBNK1 WBNK2 WBNK3 WBNK4 WBNK5 WBNK6 WBNK7

READ EXTENDED DECODER U20D (74LS138)
A4 A5 A6
REXT
RBNK0 RBNK1 RBNK2 RBNK3 RBNK4 RBNK5 RBNK6 RBNK7

C5 33/10V

U10A(74LS245)
DBUS0 DBUS1 DBUS2 DBUS3 DBUS4 DBUS5 DBUS6 DBUS7
C9 .1/50V
C4 33/10V
DIRECT
BUFEN

1.25MHz
MRSET
R27 6.81K
U10D LS132 → GPIB IN
GPIB OUT

U16D 6402 IPL
µP UART
WURT
RDATA
U18D LS00
R28 6.8K
BWRP
W DATA
U11B LS04
UPTDA (U6A-15)
C15 .1/50V

J11 DISPLAY-µ PROC.
BM/IO BR/W RBNK4 A3 A4 A5 A6 A7 RESET BUFEN RBNK7 RBNK5 BOPREQ A0 D0 A1 WBNK4 D7 D1 D5 D6 D2 A13 A14 D4 D3 COM WBNK6 A2 (ONLY TO ANALOG) BHOLD WBNK7 COM WE DISPLAY WBNK5

J1 ANALOG-µ PROC.
A2 A1 A6 A5 A3 A0 A7 A4 A8 A9 A10 COM 10MHz COM RBNK1 BHOLD WBNK3 BR/W ANAMEM RBNK3 RBNK2 WBNK2 RBNK0 D4 D3 D5 D2 D6 D1 WBNK0 D7 D0 WE ANALOG WBNK1

LAST REF DES USED												
C41	CR15	J17	P5	Q8	R78	SW1	T1	TP10	U12A	U11E	U20C	U20D	Y1

REF DES NOT USED

C19 THRU C32
CR8 THRU CR14
J3 THRU J9
J12 THRU J16
P1 THRU P4
Q1 THRU Q7
R5 THRU R11
R13 THRU R19
R76

U12A 2764 EPROM
+5V C41 .1/50V
5V A12 A7 A6 A5 A4 A3 A2 A1 A0 MD0 MD1 MD2
NC A8 A9 A11 PRQ A10 PRQ MD7 MD6 MD5 MD4 MD3

U11A SHUNT
MD0 MD1 MD2 MD3 MD4 MD5 MD6 MD7 → DBUS0 DBUS1 DBUS2 DBUS3 DBUS4 DBUS5 DBUS6 DBUS7

U18C P2114
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9
MD0 MD1 MD2 MD3
RAM
WE/RAM

U19C P2114
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9
MD4 MD5 MD6 MD7
RAM
WE/RAM

1. ALL CAPACITORS ARE IN MICROFARADS.

NOTE: UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP
K	7116	RO	2-20-84	
J	# 4651	BR	2/85	
H	# 4649	DAH	2-4-85	
G	# 3846	SC	4-20-83	
F	ECN # 3509	DC	1-6-83	
E	ECN # 2121	RO	4-15-82	

REMOVE ALL BURRS AND BREAK SHARP EDGES
DRAWN D. COOPER 1-6-78
MATERIAL
PROJ ENGR K. Ito
RELEASE APPROV 1-9-78
FINISH WAVETEK PROCESS
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± 010 ANGLES ±1° XX ± 030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: SCHEMATIC GPIB MICRO PROC

MODEL NO 175
DWG NO 0103-00-0660
REV K
CODE IDENT 23338
SHEET 1 OF 2

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U12F U13F U15Q U16Q U17Q U18Q U7F U8F	IC	74LS86	TI	8000-74-8610	8
U8Q	IC	8601/9601	FAIR	8000-86-0100	1
U17B U9C	IC	74132	TI	8007-41-3200	2
U3C	IC	74LS132	TI	8007-41-3210	1
U10B U5B U5C U6C U7C U8B	IC	74136	TI	8007-41-3600	6
U3B U4B	IC	74LS136	TI	8007-41-3610	2
U16A U2C U7Q	IC	74LS138	TI	8007-41-3810	3
U15E	IC	74151	TI	8007-41-5100	1
U11C U11D U12C	IC	74LS157	TI	8007-41-5710	3
U11B U12B U13D	IC	74161	TI	8007-41-6100	3
U14F U15F	IC	74LS161	BIQ	8007-41-6110	2
U17D	IC	74LS164	TI	8007-41-6410	1
U11Q U12Q	IC	74LS175	TI	8007-41-7510	2
U13B U14B U15B U16B	IC	74LS192	TI	8007-41-9210	4
U11E U11F U12A U12E U6A U8A	IC	74LS244	TI	8007-42-4410	6
U2F	IC	74LS245	TI	8007-42-4510	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, ARBGEN BD	1100-00-0644	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U12D	IC	74LS266	TI	8007-42-6610	1
U10A U10Q U11A U13A U14A U15A U3Q U4A U4Q U5A U5Q U6Q U7A	IC	74LS273	TI	8007-42-7310	13
U13Q U14Q	IC	74283	TI	8007-42-8300	2
U10F U9F	IC	74LS283	TI	8007-42-8310	2
U17C U17E U6B U7B	IC	74LS390	TI	8007-43-9010	4
U6E	IC, PROGRAMMED REF: 8007-44-7101	8600-00-0130	WVTK	8600-00-0130	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, ARBGEN BD	1100-00-0644	

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: PARTS LIST PCA, ARBGEN BD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO 175	DWG NO 1100-00-0644 REV E
	SCALE	CODE IDENT 23338	SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	ASSY DRWG, ARBGEN BD	0101-00-0644	WVTK	0101-00-0644	1
NONE	SCHEMATIC, ARBGEN BD	0103-00-0644	WVTK	0103-00-0644	1
C10 C11 C18 C39	CAP, CER, 10PF, 1KV	DD-100	CRL	1500-01-0011	4
C12 C14 C15 C17 C26 C30 C32 C35 C36 C38 C40 C42 C43 C46 C49 C51 C52 C53 C55 C57 C58 C59 C6 C7 C8 C9	CAP, CER, MN, .01MF, 50V	GE50-103ZA	MURAT	1500-01-0310	26
C100 C13 C16 C25 C28 C34 C41 C44 C5 C56	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z050A	CORNQ	1500-01-0405	10
C21 C22 C33	CAP, CER, 22PF, 1KV	DD-220	CRL	1500-02-2011	3
C2	CAP, CER, .0022, 1KV	DD-2228LL	CRL	1500-02-2201	1
C50 C54	CAP, CER, 33PF, 1KV	DD-330	CRL	1500-03-3011	2
C27 C3 C47	CAP, MICA, 100PF, 500V	DM15-101J	ARCO	1500-11-0100	3
C20	CAP, MICA, 56PF, 500V	DM15-560J	ARCO	1500-15-6000	1
C31 C37	CAP, ELECT, 100MF, 16V	500D1070016DC7	SPRAQ	1500-31-0101	2
C45	CAP, MYLAR, .001MF100V	225P10291WD3	SPRAQ	1500-41-0204	1
C1 C23 C24 C4 C48 C60 C61 C62 C63 C64 C65 C66 C67 C68 C69 C70 C71 C72	CAP, TANT, 22MF, 15V	196D226X9015KA1	SPRAQ	1500-72-2601	18
NONE	ARBGEN BOARD	175-0644	WVTK	1700-00-0644	1

WAVETEK PARTS LIST | TITLE: PCA, ARBGEN BD | ASSEMBLY NO. 1100-00-0644 | REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R89 R92 R94	POT, TRIM, 500	91AR500	BECK	4600-05-0104	3
R52	POT, TRIM, 5K	91AR5K	BECK	4600-05-0205	1
R79 R80 R81 R82	RES, C, 1/2W, 5%, 10	RC20GF-100	STKPL	4700-25-0100	4
R47 R61	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	2
R12 R2 R20 R25 R26 R27 R28 R29 R55 R74 R84	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	11
R1 R49 R54 R83	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	4
R70	RES, MF, 1/8W, 1%, 150	RN55D-1500F	TRW	4701-03-1500	1
R53	RES, MF, 1/8W, 1%, 15K	RN55D-1502F	TRW	4701-03-1502	1
R62 R69	RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	2
R71 R73	RES, MF, 1/8W, 1%, 21.5	RN55D-21R5F	TRW	4701-03-2159	2
R10 R13 R15 R16 R17 R18 R19 R21 R22 R23 R24 R3 R30 R4 R5 R6 R7 R8 R9	RES, MF, 1/8W, 1%, 2.21K	RN55D-2211F	TRW	4701-03-2211	19
R93 R95	RES, MF, 1/8W, 1%, 2.37K	RN55D-2371F	TRW	4701-03-2371	2
R39 R40 R56	RES, MF, 1/8W, 1%, 249	RN55D-2490F	TRW	4701-03-2490	3
R60 R66 R67 R76	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	4
R63 R64	RES, MF, 1/8W, 1%, 24.9K	RN55D-2492F	TRW	4701-03-2492	2

WAVETEK PARTS LIST | TITLE: PCA, ARBGEN BD | ASSEMBLY NO. 1100-00-0644 | REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R32 R36 R41 R42 R43	RES, SET, 5-4.99K, 1/8W QTY: 5:4701-03-4991	4789-00-0044	WVTK	4789-00-0044	1
CR14 CR15 CR18	DIODE, ZENER 6.2V	1N823A	MOT	4801-01-0823	3
CR1 CR10 CR11 CR12 CR13 CR16 CR17 CR2 CR3 CR4 CR5 CR6 CR7 CR8 CR9	DIODE	1N4148	FAIR	4807-02-6666	15
Q8	TRANS	2N2219A	NSC	4901-02-2191	1
Q5	TRANS	2N2905A	NSC	4901-02-9051	1
Q3	TRANS	2N3563	FAIR	4901-03-5630	1
Q2	TRANS	2N3640	FAIR	4901-03-6400	1
Q4	TRANS	2N3905	ITT	4901-03-9050	1
Q6	TRANS	TIP-29	TI	4902-00-0290	1
Q9	TRANS	TIP-30	TI	4902-00-0300	1
Q1	TRANS	SD215DE	SIG	4902-00-2140	1
P10	ASSY, RIBBON CABLE	922522-34-02-13	AP	6002-00-0008	1
P4	ASSY, RIBBON CABLE	922522-34-02-4.5	A/P	6002-00-0009	1
NONE	POWER BUSS BAR (ST)	6009-90-0005	WVTK	6009-90-0005	1
NONE	POWER BUS BAR	6009-90-0006	WVTK	6009-90-0006	3

WAVETEK PARTS LIST | TITLE: PCA, ARBGEN BD | ASSEMBLY NO. 1100-00-0644 | REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SKT, IC, 16PIN	DILB-16P-108	BURND	2100-03-0028	5
NONE	SOCKET, 14 PIN	C8814-01	TI	2100-03-0032	4
NONE	SPRING SOCKET	3-330-808-9	AMP	2100-03-0037	9
J19 J20 J21 J22 J23 J24 J25 J26 J27	COAX SOCKET	226287-2	AMP	2100-03-0038	9
NONE	SOCKET, 18 PIN	DIBL-18P-108	BURND	2100-03-0050	2
NONE	SOCKET, 20 PIN	DIBL-20P-108	BURND	2100-03-0051	12
NONE	TERM	200081	USECO	2100-05-0009	2
NONE	PIN, MALE	60809-2	AMP	2100-05-0020	20
NONE	TIE MOUNT	TM-256C	PANDT	2800-00-0005	3
NONE	HEAT SINK	2800-11-0002	WVTK	2800-11-0002	2
NONE	TRANSIPAD	10160	METRS	2800-11-0004	2
NONE	WASHER	B51547F015	MOT	2800-11-0015	2
K1 K2 K3 K4 K5 K6 K7	RELAY, REED, FORM-A	RA3019-1051	ETROL	4500-00-0007	7
R48	POT, TRIM, 1K	91AR1K	BECK	4600-01-0209	1
R105	POT, TRIM, 100K	91AR100K	BECK	4600-01-0402	1
R106 R107 R33 R87	POT, TRIM, 2K	91AR2K	BECK	4600-02-0201	4

WAVETEK PARTS LIST | TITLE: PCA, ARBGEN BD | ASSEMBLY NO. 1100-00-0644 | REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R45 R46 R50 R51 R85 R86	RES, MF, 1/8W, 1%, 27.4(	RN55D-2742F	TRW	4701-03-2742	6
R11 R14	RES, MF, 1/8W, 1%, 316	RN55D-3160F	TRW	4701-03-3160	2
R91	RES, MF, 1/8W, 1%, 3.32(	RN55D-3321F	TRW	4701-03-3321	1
R59	RES, MF, 1/8W, 1%, 3.65K	RN55D-3651F	TRW	4701-03-3651	1
R34	RES, MF, 1/8W, 1%, 4.02K	RN55D-4021F	TRW	4701-03-4021	1
R99	RES, MF, 1/8W, 1%, 4.32(	RN55D-4321F	TRW	4701-03-4321	1
R77 R78	RES, MF, 1/8W, 1%, 4.64(	RN55D-4641F	TRW	4701-03-4641	2
R58 R65 R98	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	3
R101 R35 R37 R38 R44 R57 R72 R75	RES, MF, 1/8W, 1%, 4.99	RN55D-4991F	TRW	4701-03-4991	8
R103	RES, MF, 1/8W, 1%, 49.9	RN55D-4992F	TRW	4701-03-4992	1
R102	RES, MF, 1/8W, 1%, 51.1	RN55D-51R1F	TRW	4701-03-5119	1
R100	RES, MF, 1/8W, 1%, 56.2	RN55D-56R2F	TRW	4701-03-5629	1
R68	RES, MF, 1/4W, 1%, 464K	RN60D-4643F	TRW	4701-13-4643	1
R104	RES, MF, 1/4W, 1%, 49.9	RN60D-49R9F	TRW	4701-13-4999	1
R96 R97	RES, MF, 1/2W, 1%, 100	RN65D-1000F	TRW	4701-23-1000	2
R31	RES MODULE 2.2K	4310R-101-222	BOURN	4770-00-0011	1

WAVETEK PARTS LIST | TITLE: PCA, ARBGEN BD | ASSEMBLY NO. 1100-00-0644 | REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	POWER BUS BAR	6009-90-0007	WVTK	6009-90-0007	3
U12H U15H U17H	IC	DAC-08EQ	AMD	7000-00-0800	3
U1H U2H	IC	LM 301AN	NSC	7000-03-0100	2
U11H U14H U4H U8H	IC	LM318H	AMD	7000-03-1800	4
U3H	IC	AD 561 J	AD	7000-05-6100	1
Q7	IC	AD 812	ANDEV	7000-08-1200	1
U5H	IC	AD 7530 KN	AD	7000-75-3000	1
U4E U5E	IC	UPD2114LC	NEC	8000-21-1400	2
U14D U16E U18E	IC	7400	TI	8000-74-0000	3
U13C U15D U17F U18F	IC	7402	TI	8000-74-0200	4
U4C	IC	74LS03	TI	8000-74-0310	1
U10C U16D U16F U2B U9Q	IC	7404	TI	8000-74-0400	5
U13E U14E	IC	74LS05	TI	8000-74-0510	2
U15C U16C	IC	7410	TI	8000-74-1000	2
U14C	IC	7474	TI	8000-74-7400	1
U7D U8C	IC	74LS74	TI	8000-74-7410	2

WAVETEK PARTS LIST | TITLE: PCA, ARBGEN BD | ASSEMBLY NO. 1100-00-0644 | REV

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE
MATERIAL	PROJ ENGR	
	RELEASE APPROV	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1 XX ±.030	
	DO NOT SCALE DWG	
	SCALE	

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: PARTS LIST PCA, ARBGEN BD

MODEL NO	DWG NO.	REV
175	1100-00-0644	E
CODE IDENT 23338	SHEET 1 OF 2	

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, REAR PANEL	0102-00-0667	WVTK	0102-00-0667	1
T1	TRANSFORMER	175-0022	WVTK	1204-00-0022	1
2	REAR PANEL	175-8380	WVTK	1400-00-8380	1
3	BRACKET	175-8913	WVTK	1400-00-8913	1
4	BRACKET, COMP SUPPORT	175-8923	WVTK	1400-00-8923	1
5	SHIELD, PLASTIC	175-8940	WVTK	1400-00-8940	1
6	END BELL, CHROME	175-9010	WVTK	1400-00-9010	1
1	I.D. LABEL	801-9090	WVTK	1400-00-9090	1
19	POLYESTER FILM REF: 1600-99-0002	175-3191	WVTK	1400-01-3191	1
C2 C3	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z050A	CORNO	1500-01-0405	2
C1	CAP, ELEC, 52000MF, 15V	FAHM52000-15-83	CDE	1500-35-2301	1
7	BNC CONN	KC-7946	KING	2100-01-0002	9
J14	CONN, 9PIN	03-06-1091	MOLEX	2100-02-0010	1
J1	CONN, 15PIN	03-09-1151	MOLEX	2100-02-0012	1
S1	RECEPTACLE	6WJ1	CORCM	2100-03-0026	1
NONE	CABLE CONTACT	226286-2	AMP	2100-03-0040	9

WAVETEK PARTS LIST	TITLE: REAR PANEL	ASSEMBLY NO. 1101-00-0667	REV H
		PAGE 1	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
9	SOLDER LUG	1497	SMITH	2100-04-0012	9
8	SOLDER LUG	11A144	ZIER	2100-04-0025	2
NONE	PIN, FEMALE	02-06-1103	MOLEX	2100-05-0002	5
NONE	PIN, FEMALE	02-09-1118	MOLEX	2100-05-0026	5
NONE	CONNECTOR PIN	350415-1	AMP	2100-05-0039	2
F1	FUSE, 2A, 250V	312002	LITFU	2400-05-0022	1
NONE	TIE STRAP	SST-1.5M	PANDT	2800-00-0003	4
11	STANDOFF SHAGE, 1/4 HEX, 0.062 MATL	BR6921B-0.437-31	LNTRN	2800-05-0007	5
12	INSERT # 6	74-11-106-13	SOTCO	2800-09-0017	6
13	INSERT #8	74-11-108-13	SOTCO	2800-09-0018	1
14	INSERT #10	74-11-210-13	SOTCO	2800-09-0026	1
15	GROMMET, RUBBER	2172	SMITH	2800-10-0006	1
16	CAP, MTG, BKT	FJMR	STM	2800-12-0006	1
	RIVET 1/8X3/16L	1125-0406	AVDEL	2800-12-0011	2
NONE	WASHER, SHOULDER	2668	SMITH	2800-27-0004	9
NONE	NYLON FLAT WASHER	2264-N-385	AMTOM	2800-28-0003	9

WAVETEK PARTS LIST	TITLE: REAR PANEL	ASSEMBLY NO. 1101-00-0667	REV H
		PAGE 2	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
17	PLUG BUTTON	48152	UNCAR	2800-35-0001	2
V1	VARISTOR	4899-00-0043	WVTK	4799-00-0048	1
CR1	BRIDGE ASSY 30 AMP	MDA990-1	MOT	4899-00-0010	1
NONE	WIRE, COAX	BTX019-10050	BRKTC	6001-40-0005	14
NONE	PWR CORD	6001-80-0005	WVTK	6001-80-0005	1

WAVETEK PARTS LIST	TITLE: REAR PANEL	ASSEMBLY NO. 1101-00-0667	REV H
		PAGE 3	

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST REAR PANEL
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 175 / DWG NO 1101-00-0667 / REV H
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO A-3894

APPENDIX A

American Standard Code for Information Interchange (ASCII)

Binary													
			Bit 7		0	0	0	0	1	1	1	1
			Bit 6		0	0	1	1	0	0	1	1
			Bit 5		0	1	0	1	0	1	0	1
Bit 4	Bit 3	Bit 2	Bit 1	Hex	0	1	2	3	4	5	6	7
0	0	0	0	0	NUL	DLE	SP	0	@	P	\	p
0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	2	STX	DC2	"	2	B	R	b	r
0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
1	0	0	0	8	BS	CAN	(	8	H	X	h	x
1	0	0	1	9	HT	EM	)	9	I	Y	i	y
1	0	1	0	A	LF	SUB	*	:	J	Z	j	z
1	0	1	1	B	VT	ESC	+	;	K	[	k	[
1	1	0	0	C	FF	FS	,	<	L	\	l	:
1	1	0	1	D	CR	GS	–	=	M	]	m	]
1	1	1	0	E	SO	RS	.	>	N	↑	n	~
1	1	1	1	F	S1	US	/	?	O	←	o	DEL

NUL = All zeros
SOH = Start of heading
STX = Start of text
EOT = End of transmission
ENQ = Enquiry
ACK = Acknowledgement
BEL = Bell or attention signal
BS = Back space
HT = Horizontal tabulation
LF = Line feed
VT = Vertical tabulation
FF = Form feed
CR = Carriage return
SO = Shift out
S1 = Shift in
DLE = Data link escape
DC 1 = Device control 1
DC 2 = Device control 2
DC 3 = Device control 3
DC 4 = Device control 4
NAK = Negative acknowledgement
SYN = Synchronous/idle
ETB = End of transmitted block
CAN = Cancel (error in data)
EM = End of medium
SUB = Start of special sequence
ESC = Escape
FS = Information file separator
GS = Information group separator
RS = Information record separator
US = Information unit separator
DEL = Delete

For GPIB:

DC4	=	DCL	Device clear	Universal Command Group
DC1	=	LLO	Local lockout	
NAK	=	PPU	Parallel poll unconfigure	
EM	=	SPD	Serial poll disable	
CAN	=	SPE	Serial poll enable	
SOH	=	GTL	Go to local	Address Command Group
EOT	=	SDC	Selected device clear	
ENQ	=	PPC	Parallel poll configure	
PS	=	GET	Group execute trigger	
HT	=	TCT	Take control	

APPENDIX B

Programming Examples

The following two programs demonstrate the use of various features of the Arb's GPIB interface. They are written in Tektronix 4051 BASIC and HP9830 BASIC, but can be easily adapted to other BASICs by changing the PRINT statements to be compatible with the style of GPIB bus addressing in the other BASIC, and by replacing the CMD and WBYTE statements with equivalent programming.

B.1 Example 1 Bursts of 300 Cycles of Increasing Frequency (from 1 kHz to 2 kHz)

This program uses the SRQ on transition-to-holding capability to sense when a burst is completed, so it can start the next burst within 10 ms.

HP9830 Controller

```
1000 REM INITIALIZE ARB TO POWER-ON CONDITIONS BY SENDING A "Z".
1010 REM THE ARB'S ADDRESS MUST BE SET TO 4 FOR THIS PROGRAM.
1020 REM IN THE CMD STATEMENTS, THE FIRST STRING CONTAINS GPIB ADDRESSING
1030 REM INFORMATION. "?" IS AN UNLISTEN COMMAND, "U" IS THE CALCULATOR'S
1040 REM TALK ADDRESS, AND "$" IS THE ARB'S LISTEN ADDRESS.
1050 CMD "?U$","Z"
1060 REM AFTER SENDING A "Z" IT IS NECESSARY TO WAIT ABOUT 3 MS TO INSURE
1070 REM THAT THE FOLLOWING COMMANDS WILL NOT BE LOST.  THIS IS DONE BY
1080 REM INITIALIZING THE FREQUENCY VARIABLE F.
1090 F=1100
1100 REM SET UP ARB PARAMETERS FOR TRIGGERED BURST OPERATION.
1110 REM SET TRIGGERED MODE, SET PRESET LENGTH TO 300, TURN OUTPUT ON, SET
1120 REM FREQUENCY TO 1KHZ, AND SET SRQ ENABLE CODE TO ALLOW THE SRQ TO BE
1130 REM TURNED ON WHEN THE BURST STOPS.
1140 CMD "?U$","B1L300P1F1000Q2I"
1150 REM START OF LOOP.
1160 REM FIRST SEND A GET COMMAND.  NOTE THAT THE ARB IS ALREADY ADDRESSED
1170 REM TO LISTEN, SO IT IS ONLY NECESSARY TO SEND THE GET CODE (8).
1180 OUTPUT (13,1190)256,8,512;
1190 FORMAT 3B
1200 REM NEXT DO A SERIAL POLL TO TURN SRQ OFF. NOTE THAT THIS AND ALL THE
1210 REM FOLLOWING STATEMENTS ARE DONE WHILE THE ARB IS OUTPUTTING THE TRIGGERED
1220 REM BURST.
1230 REM SEND SPE.
1240 OUTPUT (13,1190)256,24,512;
1250 REM ADDRESS ARB TO TALK, CALCULATOR TO LISTEN.
1260 CMD "?D5"
1270 REM READ STATUS BYTE
1280 P=RBYTE13
1290 REM ADDRESS ARB TO LISTEN AND CALCULATOR TO TALK.
1300 CMD "?U$"
1310 REM SEND SPD.
1320 OUTPUT (13,1190)256,25,512;
1330 REM NEXT SEND THE NEXT FREQUENCY IN SEQUENCE.  NOTE THAT SINCE NO EXECUTE
1340 REM IS DONE, THIS NEW FREQUENCY WILL NOT ACTUALLY BE PROGRAMMED INTO THE
1350 REM WAVEFORM CIRCUITS UNTIL THE GROUP EXECUTE TRIGGER AT STATEMENT 1180
1360 REM IS DONE.
1370 OUTPUT (13,*)"F";F
1380 REM COMPUTE NEXT FREQUENCY.
1390 F=F+100
1400 IF F<2100 THEN 1430
1410 F=1000
1420 REM FINALLY WAIT FOR SRQ TO COME ON, SIGNALLING THE END OF THE BURST.
1430 IF STAT13>1 THEN 1430
1440 GOTO 1180
```

Tektronix 4051 Controller

```
1000 REM ARRAYS A AND B HOLD SINE AND COSINE COEFFICIENTS, Y HOLDS
1010 REM THE WAVEFORM MEMORY Y VALUES.
1020 DIM A(7), B(7), Y(256)
1030 REM THE ARB'S ADDRESS MUST BE SET TO 4 FOR THIS PROGRAM.
1040 REM FIRST INITIALIZE CALCUALTOR AND ARB. THE "@4:" IN THE
1050 REM PRINT STATEMENT IS THE ARB'S ADDRESS.
1060 SET RADIAN
1070 PRINT @4: "A5DØBØP1O1T2E-5UØC8IXØ"
1080 REM CLEAR SCREEN
1090 PAGE
1100 FOR C=1 TO 7
1110 A(C)=0
1120 B(C)=0
1130 NEXT C
1140 REM READ SINE AND COSINE COEFFICIENTS FROM USER.
1150 PRINT "ENTER SINE COEFFICIENTS A(1), A(2),...,A(7)"
1160 REM THE FOLLOWING STATEMENT READS IN ALL 7 VALUES
1170 INPUT A
1180 PRINT "ENTER COSINE COEFFICIENTS B(1),B(2),...,B(7)"
1190 INPUT B
1200 REM D HOLDS NUMBER OF RADIANS PER ARB MEMORY CELL.
1210 D=2*PI/256
1220 REM M HOLDS MAXIMUM VALUE OF WAVEFORM AMPLITUDE.
1230 REM THIS WILL BE USED LATER TO SCALE THE WAVEFORM
1240 REM TO FIT WITHIN THE ARB LIMITS (-127 TO 127).
1250 M=0
1260 REM COMPUTE WAVEFORM. X SELECTS THE ARB WAVEFORM
1270 REM MEMORY CELL FOR WHICH A VALUE IS BEING COMPUTED.
1280 FOR X=Ø TO 255
1290 REM T IS THE ANGLE FOR MEMORY CELL X IN RADIANS.
1300 T=X*D
1310 E=Ø
1320 FOR C=1 TO 7
1330 E=E+A(C)*SIN(C*T)+B(C)*COS(C*T)
1340 NEXT C
1350 REM TEST IF POINT JUST COMPUTED HAS A LARGER ABSOLUTE
1360 REM VALUE THAN ANY PREVIOUS POINT.
1370 IF ABS(E)=M THEN 14ØØ
1380 REM IF SO, SET M TO NEW MAXIMUM
1390 M=ABS(E)
1400 Y(X+1)=E
1410 NEXT X
1420 REM COMPUTE SCALING FACTOR WHICH WILL ADJUST THE
1430 REM VALUES IN THE Y ARRAY SO THEY WILL VARY BETWEEN
1440 REM -12Ø TO 12Ø
1450 S=120/M
1460 REM WRITE Y-VALUE TO ARB. THIS LOOP USES THE
1470 REM AUTO-INCREMENT FEATURE OF THE Y PARAMETER TO
1480 REM ACHIEVE MAXIMUM SPEED. AFTER EACH Y VALUE IS
1490 REM ACCEPTED BY THE ARB, THE ARB'S X PARAMETER IS
1500 REM AUTOMATICALLY INCREMENTED TO POINT TO THE
1510 REM NEXT WAVEFORM MEMORY CELL. THE X PARAMETER
1520 REM WAS INITIALIZED TO ZERO IN STATEMENT 1Ø7Ø.
1530 FOR X=1 TO 256
1540 PRINT @1: "Y"; Y(X)*S
1550 NEXT X
1560 60 TO 1090
```

APPENDIX C

PERMANENT CUSTOM WAVEFORMS

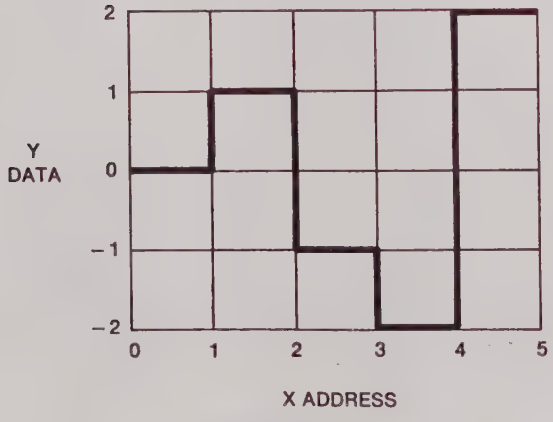
Four 74S471 PROMs containing custom waveform data may be added in socket positions U7E through U10E on the generator board 1100-00-0644 (drawing 0101-00-0644). Each of the 256 PROM addresses may be encoded for one of 255 values. Consult the manufacturer's literature for 74S471 PROM encoding.

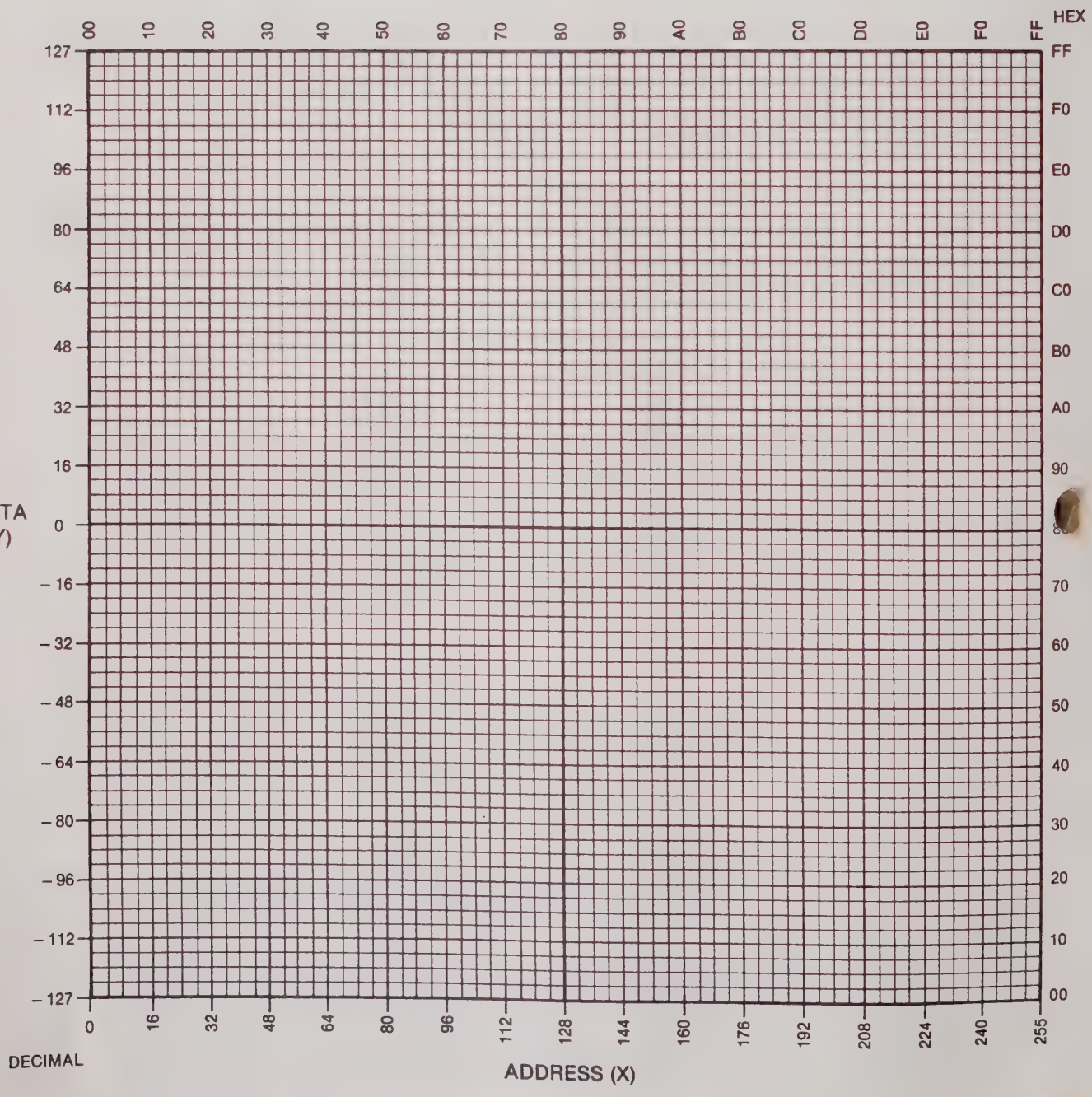
Refer to paragraph 3.2.2(19) for operator access to these waveforms.

Approach

Use a copy of figure C-1 to sketch your custom waveform and transfer the data points to a copy of table C-1. (Table C-2 is a fast reference to convert each address or data point to hexadecimal code.) An example of programming is shown below.

X Address Value	Y Data Value
00	80
01	81
02	7F
03	7E
04	82





This grid may be reproduced and used for waveform sketching and planning.

Table C-1. PROM Programming Worksheet

X DEC	X HEX	Y DEC	Y HEX
0	00		
1	01		
2	02		
3	03		
4	04		
5	05		
6	06		
7	07		
8	08		
9	09		
10	0A		
11	0B		
12	0C		
13	0D		
14	0E		
15	0F		
16	10		
17	11		
18	12		
19	13		
20	14		
21	15		
22	16		
23	17		
24	18		
25	19		
26	1A		
27	1B		
28	1C		
29	1D		
30	1E		
31	1F		
32	20		
33	21		
34	22		
35	23		
36	24		
37	25		
38	26		
39	27		

X DEC	X HEX	Y DEC	Y HEX
40	28		
41	29		
42	2A		
43	2B		
44	2C		
45	2D		
46	2E		
47	2F		
48	30		
49	31		
50	32		
51	33		
52	34		
53	35		
54	36		
55	37		
56	38		
57	39		
58	3A		
59	3B		
60	3C		
61	3D		
62	3E		
63	3F		
64	40		
65	41		
66	42		
67	43		
68	44		
69	45		
70	46		
71	47		
72	48		
73	49		
74	4A		
75	4B		
76	4C		
77	4D		
78	4E		
79	4F		

X DEC	X HEX	Y DEC	Y HEX
80	50		
81	51		
82	52		
83	53		
84	54		
85	55		
86	56		
87	57		
88	58		
89	59		
90	5A		
91	5B		
92	5C		
93	5D		
94	5E		
95	5F		
96	60		
97	61		
98	62		
99	63		
100	64		
101	65		
102	66		
103	67		
104	68		
105	69		
106	6A		
107	6B		
108	6C		
109	6D		
110	6E		
111	6F		
112	70		
113	71		
114	72		
115	73		
116	74		
117	75		
118	76		
119	77		

X DEC	X HEX	Y DEC	Y HEX
120	78		
121	79		
122	7A		
123	7B		
124	7C		
125	7D		
126	7E		
127	7F		
128	80		
129	81		
130	82		
131	83		
132	84		
133	85		
134	86		
135	87		
136	88		
137	89		
138	8A		
139	8B		
140	8C		
141	8D		
142	8E		
143	8F		
144	90		
145	91		
146	92		
147	93		
148	94		
149	95		
150	96		
151	97		
152	98		
153	99		
154	9A		
155	9B		
156	9C		
157	9D		
158	9E		
159	9F		

Table C-1. PROM Programming Worksheet (Continued)

X DEC	X HEX	Y DEC	Y HEX
160	A0		
161	A1		
162	A2		
163	A3		
164	A4		
165	A5		
166	A6		
167	A7		
168	A8		
169	A9		
170	AA		
171	AB		
172	AC		
173	AD		
174	AE		
175	AF		
176	B0		
177	B1		
178	B2		
179	B3		
180	B4		
181	B5		
182	B6		
183	B7		

X DEC	X HEX	Y DEC	Y HEX
184	B8		
185	B9		
186	BA		
187	BB		
188	BC		
189	BD		
190	BE		
191	BF		
192	C0		
193	C1		
194	C2		
195	C3		
196	C4		
197	C5		
198	C6		
199	C7		
200	C8		
201	C9		
202	CA		
203	CB		
204	CC		
205	CD		
206	CE		
207	CF		

X DEC	X HEX	Y DEC	Y HEX
208	D0		
209	D1		
210	D2		
211	D3		
212	D4		
213	D5		
214	D6		
215	D7		
216	D8		
217	D9		
218	DA		
219	DB		
220	DC		
221	DD		
222	DE		
223	DF		
224	E0		
225	E1		
226	E2		
227	E3		
228	E4		
229	E5		
230	E6		
231	E7		

X DEC	X HEX	Y DEC	Y HEX
232	E8		
233	E9		
234	EA		
235	EB		
236	EC		
237	ED		
238	EE		
239	EF		
240	F0		
241	F1		
242	F2		
243	F3		
244	F4		
245	F5		
246	F6		
247	F7		
248	F8		
249	F9		
250	FA		
251	FB		
252	FC		
253	FD		
254	FE		
255	FF		

Table C-2. X (Address)-to-Hex and Y (Data or Position)-to-Hex Conversion Table

X	Y	HEX
0		00
1	−127	01
2	−126	02
3	−125	03
4	−124	04
5	−123	05
6	−122	06
7	−121	07
8	−120	08
9	−119	09
10	−118	0A
11	−117	0B
12	−116	0C
13	−115	0D
14	−114	0E

X	Y	HEX
15	−113	0F
16	−112	10
17	−111	11
18	−110	12
19	−109	13
20	−108	14
21	−107	15
22	−106	16
23	−105	17
24	−104	18
25	−103	19
26	−102	1A
27	−101	1B
28	−100	1C
29	−99	1D

X	Y	HEX
30	−98	1E
31	−97	1F
32	−96	20
33	−95	21
34	−94	22
35	−93	23
36	−92	24
37	−91	25
38	−90	26
39	−89	27
40	−88	28
41	−87	29
42	−86	2A
43	−85	2B
44	−84	2C

X	Y	HEX
45	−83	2D
46	−82	2E
47	−81	2F
48	−80	30
49	−79	31
50	−78	32
51	−77	33
52	−76	34
53	−75	35
54	−74	36
55	−73	37
56	−72	38
57	−71	39
58	−70	3A
59	−69	3B

Table C-2. X (Address)-to-Hex and Y (Data or Position)-to-Hex Conversion Table (Continued)

X	Y	HEX	X	Y	HEX	X	Y	HEX	X	Y	HEX
60	−68	3C	109	−19	6D	158	30	9E	207	79	CE
61	−67	3D	110	−18	6E	159	31	9F	208	80	D0
62	−66	3E	111	−17	6F	160	32	A0	209	81	D1
63	−65	3F	112	−16	70	161	33	A1	210	82	D2
64	−64	40	113	−15	71	162	34	A2	211	83	D3
65	−63	41	114	−14	72	163	35	A3	212	84	D4
66	−62	42	115	−13	73	164	36	A4	213	85	D5
67	−61	43	116	−12	74	165	37	A5	214	86	D6
68	−60	44	117	−11	75	166	38	A6	215	87	D7
69	−59	45	118	−10	76	167	39	A7	216	88	D8
70	−58	46	119	−9	77	168	40	A8	217	89	D9
71	−57	47	120	−8	78	169	41	A9	218	90	DA
72	−56	48	121	−7	79	170	42	AA	219	91	DB
73	−55	49	122	−6	7A	171	43	AB	220	92	DC
74	−54	4A	123	−5	7B	172	44	AC	221	93	DD
75	−53	4B	124	−4	7C	173	45	AD	222	94	DE
76	−52	4C	125	−3	7D	174	46	AE	223	95	DF
77	−51	4D	126	−2	7E	175	47	AF	224	96	E0
78	−50	4E	127	−1	7F	176	48	B0	225	97	E1
79	−49	4F	128	0	80	177	49	B1	226	98	E2
80	−48	50	129	1	81	178	50	B2	227	99	E3
81	−47	51	130	2	82	179	51	B3	228	100	E4
82	−46	52	131	3	83	180	52	B4	229	101	E5
83	−45	53	132	4	84	181	53	B5	230	102	E6
84	−44	54	133	5	85	182	54	B6	231	103	E7
85	−43	55	134	6	86	183	55	B7	232	104	E8
86	−42	56	135	7	87	184	56	B8	233	105	E9
87	−41	57	136	8	88	185	57	B9	234	106	EA
88	−40	58	137	9	89	186	58	BA	235	107	EB
89	−39	59	138	10	8A	187	59	BB	236	108	EC
90	−38	5A	139	11	8B	188	60	BC	237	109	ED
91	−37	5B	140	12	8C	189	61	BD	238	110	EE
92	−36	5C	141	13	8D	190	62	BE	239	111	EF
93	−35	5D	142	14	8E	191	63	BF	240	112	F0
94	−34	5E	143	15	8F	192	64	C0	241	113	F1
95	−33	5F	144	16	90	193	65	C1	242	114	F2
96	−32	60	145	17	91	194	66	C2	243	115	F3
97	−31	61	146	18	92	195	67	C3	244	116	F4
98	−30	62	147	19	93	196	68	C4	245	117	F5
99	−29	63	148	20	94	197	69	C5	246	118	F6
100	−28	64	149	21	95	198	70	C6	247	119	F7
101	−27	65	150	22	96	199	71	C7	248	120	F8
102	−26	66	151	23	97	200	72	C8	249	121	F9
103	−25	67	152	24	98	201	73	C9	250	122	FA
104	−24	68	153	25	99	202	74	CA	251	123	FB
105	−23	69	154	26	9A	203	75	CB	252	124	FC
106	−22	6A	155	27	9B	204	76	CC	253	125	FD
107	−21	6B	156	28	9C	205	77	CD	254	126	FE
108	−20	6C	157	29	9D	206	78	CE	255	127	FF

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